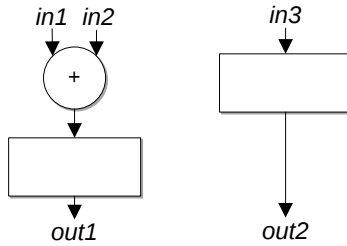
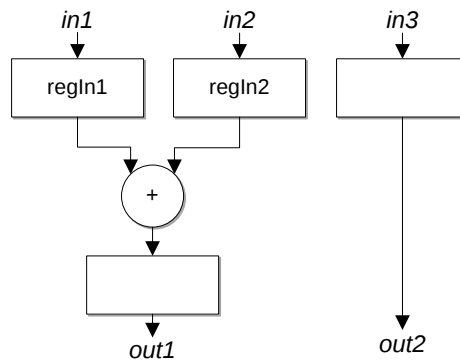


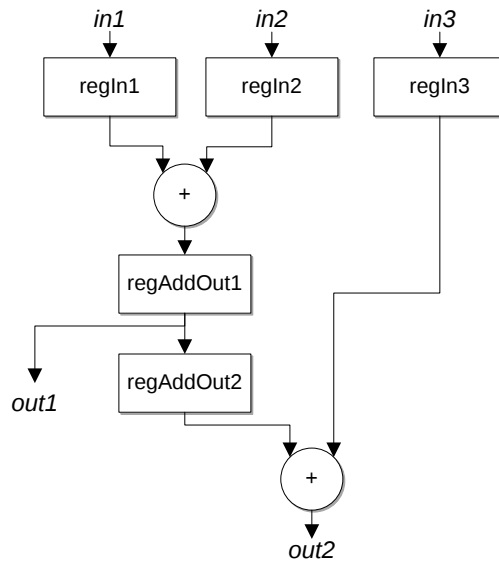
ARCH1



ARCH2



ARCH3



KEY: All rectangles are registers. All wires are *width* bits, where *width* is a VHDL generic. All register names correspond to internal signal names in the VHDL. Note that registers that are *only* connected to outputs do not require internal signals and therefore have no name shown.