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Gregory Stitt

Research Interests

Reconfigurable computing: emphasis in design automation, synthesis, compilers, embedded systems, hardware/software co-design, low power-design, system-on-a-chip multi-core architectures, and run-time optimizations.

Education

- Ph.D. Computer Science, University of California, Riverside, June 2007, Thesis title: *Synthesis From Software Binaries: An Enabling Technology for Dynamic and Transparent Synthesis*, Advisor: Dr. Frank Vahid
- B.S. Computer Science, University of California, Riverside, June 2000, GPA: 3.953, Summa Cum Laude

Employment

- Associate Professor, University of Florida, Department of Electrical and Computer Engineering, August 2013 to current
- Assistant Professor, University of Florida, Department of Electrical and Computer Engineering, August 2007 to August 2013

Teaching

- EEL4712 (Digital Design) – Assistant/Associate Professor, UF (Spring 2010-2017)
- EEL5721/EEL4720 (Reconfigurable Computing) – Assistant/Associate Professor, UF (Fall 2012-2016)
- EEL4930/EEL5934 (Reconfigurable Computing) – Assistant Professor, UF (Fall 2007-2011, Spring 2008-2009)
- CS 161L (Computer Architecture) – Lecturer, UCR (Spring 2005)
- CS 161 (Computer Architecture) - Teaching assistant, UCR (Fall 2001)
- CS 122A (Embedded Systems) - Teaching assistant, UCR (Fall 2000, 2003)
- CS 122B (Adv. Embedded Systems) - Teaching assistant, UCR (Winter 2003, 2004)
- Computer science tutor, UCR Learning Center (1999)

Patents

[1] G. Stitt, D. Campbell, R. Aloni, T. Vaseliou, J. Salkey. Architecture-Independent Approximation Discovery. Serial No. 62/527,667; filed June 30, 2017. UF#-16791

[2] K. Yang. K. Robert, S. Bhunia, G. Stitt. A Uniquified FPGA Virtualization Approach to Hardward Security, Filed 12/13/2016, UF# 16477

[3] J. Coole and G. Stitt. Overlay Architecture For Programing FPGAs. Filed 4/29/2016, U.S. Provisional App. No.: 62/329,944; UF# 16190

[4] G. Stitt and J. Wernsing. Elastic Computing, filed 04/11/11, UF#-13728, 222106-8135, Patent Application Serial No. 61/474,020.

[5] F. Vahid, R. Lysecky, and G. Stitt. Warp processor for dynamic hardware/software partitioning, 2008, US Patent 7,356,672.

Journal Publications

[1] A. Landy and G. Stitt, "Serial arithmetic strategies for improving fpga throughput," *ACM Trans. Embed. Comput. Syst.*, vol. 16, pp. 84:1–84:25, July 2017.

[2] G. Stitt, R. Karam, K. Yang, and S. Bhunia, "A uniquified virtualization approach to hardware security," *IEEE Embedded Systems Letters*, vol. 9, pp. 53-56, September 2017.

[3] D. Wilson and G. Stitt, "A scalable, low-overhead finite-state machine overlay for rapid FPGA application development," *CoRR*, vol. abs/1705.02732, February 2017.

[4] G. Stitt, E. Schwartz, and P. Cooke, "A parallel sliding-window generator for high-performance digital-signal processing on fpgas," *ACM Trans. Reconfigurable Technol. Syst.*, vol. 9, pp. 23:1–23:22, May 2016.

[5] D. Wilson and G. Stitt, "The unified accumulator architecture: A configurable, portable, and extensible floating-point accumulator," *ACM Trans. Reconfigurable Technol. Syst.*, vol. 9, pp. 21:1–21:23, May 2016.

[6] G. Wang, G. Stitt, H. Lam, and A. George, "Core-level modeling and frequency prediction for dsp applications on fpgas," *International Journal of Rec*, p. 20, 2015.
[7] R. Kirchgessner, A. D. George, and G. Stitt, "Low-overhead fpga middleware for application portability and productivity," *ACM Trans. Reconfigurable Technol. Syst.*, vol. 8, pp. 21:1–21:22, September 2015.
[8] P. Cooke, J. Fowers, G. Brown, and G. Stitt, "A tradeoff analysis of fpgas, gpus, and multicores for sliding-window applications," *ACM Transactions on Reconfigurable Technology and Systems (TRETS)*, vol. 8, pp. 2:1–2:24, Mar 2015.
[9] P. Cooke, L. Hao, and G. Stitt, "Finite-state-machine overlay architectures for fast fpga compilation and application portability," *ACM Transactions on Embedded Computing Systems (TECS)*, vol. 1, p. 25, 2014.
[10] J. Coole and G. Stitt, "Fast, flexible high-level synthesis from opencl using reconfiguration contexts," *Micro, IEEE*, vol. 34, pp. 42-53, Jan 2014.
[11] J. Fowers, G. Brown, J. Wernsing, and G. Stitt, "A performance and energy comparison of convolution on GPUs, FPGAs, and multicore processors," *ACM Transactions on Architecture and Code Optimization (TACO) - Special Issue on High-Performance Embedded Architectures and Compilers*, vol. 9, pp. 25:1–25:21, January 2013.
[12] L. Hao and G. Stitt, "Bandwidth-sensitivity-aware arbitration for FPGAs," *Embedded Systems Letters, IEEE*, vol. 4, pp. 73-76, September 2012.
[13] J. R. Wernsing and G. Stitt, "Elastic computing: A portable optimization framework for hybrid computers," *Parallel Computing*, vol. 38, pp. 438–464, August 2012.
[14] C. Reardon, B. Holland, A. D. George, G. Stitt, and H. Lam, "Rcml: An environment for estimation modeling of reconfigurable computing systems," *ACM Transactions on Embedded Computing Systems (TECS): Special Section on CAPA'09*, vol. 11, pp. 43:1–43:22, August 2012.
[15] A. George, H. Lam, and G. Stitt, "Novo-g: at the forefront of scalable reconfigurable supercomputing," *IEEE Computing in Science and Engineering Magazine*, pp. 82–86, Jan/Feb 2011.
[16] G. Stitt, A. George, H. Lam, M. Smith, V. Aggarwal, G. Wang, C. Reardon, B. Holland, S. Koehler, and J. Coole, "An end-to-end tool flow for FPGA-accelerated scientific computing," *IEEE Design&Test of Computers: Special Issue on Design Methods and Tools for FPGA-Based Acceleration of Scientific Computing*, vol. 28, pp. 68-77, July/August 2011.
[17] G. Stitt, "Are field-programmable gate arrays ready for the mainstream? ," *Micro, IEEE*, vol. 31, pp. 58-63, Nov/Dec 2011.
[18] G. Stitt and J. Coole, "Intermediate fabrics: Virtual architectures for near-instant FPGA compilation," *Embedded Systems Letters, IEEE*, vol. 3, pp. 81 -84, sept. 2011.
[19] J. Curreri, G. Stitt, and A. George, "High-level synthesis of in-circuit assertions for verification, debugging, and timing analysis," *International Journal of Reconfigurable Computing*, vol. 2011, pp. 1-17, December 2011.
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[22] G. Stitt and F. Vahid, "Thread warping: Dynamic and transparent synthesis of thread accelerators," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, vol. 16, pp. 32:1–32:21, June 2011.
[23] J. Coole and G. Stitt, "Traversal caches: A framework for FPGA acceleration of pointer data structures," *International Journal of Reconfigurable Computing*, vol. 2010, pp. 1-16, December 2010.
[24] F. Vahid, G. Stitt, and R. Lysecky, "Warp processing: Dynamic translation of binaries to FPGA circuits," *Computer*, vol. 41, pp. 40-46, July 2008.
[25] G. Stitt and F. Vahid, "Binary synthesis," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, vol. 12, pp. 1–30, August 2007.
[26] R. Lysecky, G. Stitt, and F. Vahid, "Warp processors," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, vol. 11, pp. 659–681, June 2006.
[27] G. Stitt, F. Vahid, and S. Nematbakhsh, "Energy savings and speedups from partitioning critical software loops to hardware in embedded systems," *ACM Transactions on Embedded Computing Systems (TECS)*, vol. 3, pp. 218–232, February 2004.
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[29] J. Villarreal, D. Suresh, G. Stitt, F. Vahid, and W. Najjar, "Improving software performance with configurable logic," *Kluwer Journal on Design Automation of Embedded Systems*, vol. 7, pp. 325–339, November 2002.
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[31] F. Vahid, R. Patel, and G. Stitt, "Propagating constants past software to hardware peripherals in fixed-application embedded systems," *ACM SIGARCH Computer Architecture News*, vol. 29, pp. 25–30, December 2001. Selected for special issue from earlier version of paper in Compilers and Operating Systems for Low Power (COLP'01).

Book Chapters

[1] F. Vahid and G. Stitt. *Reconfigurable Computing: The Theory and Practice of FPGA-Based Computation.* Morgan Kaufmann, 2007, ch. (26) Hardware/Software Partitioning, pp. 539–560.
[2] G. Stitt and F. Vahid. *Compilers and operating systems for low power*. Kluwer Academic Publishers, 2003, ch. Propagating

Constants Past Software to Hardware Peripherals in Fixed-Application Embedded Systems, pp. 115–135.

Conference Publications

[1] M. N. Emas, A. Baylis, and G. Stitt, "High-frequency absorption-fifo pipelining for stratix 10 hyperflex," in *The 26th IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, April 2018.

[2] G. Stitt, A. Gupta, M. N. Emas, D. Wilson, and A. Baylis, "Scalable window generation for the intel broadwell+arria 10 and high-bandwidth fpga systems," in *Proceedings of the 2018 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays*, FPGA '18, pp. 173–182, February 2018.

[3] C. Pascoe, S. Chenna, G. Stitt, and H. Lam, "A fpga-pipelined approach for accelerated discrete-event simulation of hpc systems," in *Heterogeneous High-performance Reconfigurable Computing (H2RC)*, p. 2, November 2017.

[4] A. Baylis, G. Stitt, and A. Gordon-Ross, "Overlay-based side-channel countermeasures: A case study on correlated noise generation," in *2017 IEEE 60th International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 1308-1311, August 2017.

[5] D. Wilson and G. Stitt, "A scalable, low-overhead finite-state machine overlay for rapid fpga application development," in *International Workshop on Overlay Architectures for FPGAs (OLAF), co-located with FPGA 2017*, February 2017.

[6] N. Kumar, C. Pascoe, C. Hajas, H. Lam, G. Stitt, and A. George, "Behavioral emulation for scalable design-space exploration of algorithms and architectures," in *International Conference on High Performance Computing*, pp. 5-17, 2016.

[7] C. Pascoe, N. Kumar, H. Lam, and G. Stitt, "Fpga-pipelined discrete-event simulations for accelerated behavioral emulation of extreme-scale systems," in *Workshop on Modeling & Simulation of Systems & Applications (ModSim)*, 2016.

[8] N. Kumar, A. George, H. Lam, G. Stitt, and S. Hammond, "Understanding performance and reliability trade-offs for extreme-scale systems using behavioral emulation," in *Workshop on Modeling & Simulation of Systems and Applications (ModSim)*, 2015.

[9] A. Shastri, G. Stitt, and E. Riccio, "A scheduling and binding heuristic for high-level synthesis of fault-tolerant fpga applications," in *Application-specific Systems, Architectures and Processors (ASAP), 2015 IEEE 26th International Conference on*, pp. 202-209, July 2015.

[10] D. Rudolph and G. Stitt, "An interpolation-based approach to multi-parameter performance modeling for heterogeneous systems," in *Application-specific Systems, Architectures and Processors (ASAP), 2015 IEEE 26th International Conference on*, pp. 174-180, July 2015.

[11] J. Coole and G. Stitt, "Adjustable-cost overlays for runtime compilation," in *Field-Programmable Custom Computing Machines (FCCM), 2015 IEEE 23rd Annual International Symposium on*, pp. 21-24, May 2015.

[12] A. Landy and G. Stitt, "Revisiting serial arithmetic: A performance and tradeoff analysis for parallel applications on modern fpgas," in *Field-Programmable Custom Computing Machines (FCCM), 2015 IEEE 23rd Annual International Symposium on*, pp. 9-16, May 2015.

[13] J. Fowers, J. Liu, and G. Stitt, "A framework for dynamic parallelization of fpga-accelerated applications," in *Proceedings of the 17th International Workshop on Software and Compilers for Embedded Systems*, SCOPES '14, pp. 1–10, 2014.

[14] J. Fowers, K. Ovtcharov, K. Strauss, E. S. Chung, and G. Stitt, "A high memory bandwidth fpga accelerator for sparse matrix-vector multiplication," in *Proceedings of the 2014 IEEE 22nd International Symposium on Field-Programmable Custom Computing Machines*, FCCM '14, pp. 36–43, 2014.

[15] J. Coole and G. Stitt, "Opencl high-level synthesis for mainstream fpga acceleration," in *Workshop on SoCs, Heterogeneous Architectures and Workloads (SHAW)*, feb 2014.

[16] A. Landy and G. Stitt, "Pseudo-constant logic optimization," in *Application-Specific Systems, Architectures and Processors (ASAP), 2013 IEEE 24th International Conference on*, pp. 99-102, June 2013.

[17] P. Cooke, J. Fowers, G. Stitt, and L. Hunt, "A comparison of correntropy-based feature tracking on fpgas and gpus," in *Application-Specific Systems, Architectures and Processors (ASAP), 2013 IEEE 24th International Conference on*, pp. 237-240, June 2013.

[18] L. Hao and G. Stitt, "Virtual finite-state-machine architectures for fast compilation and portability," in *Application-Specific Systems, Architectures and Processors (ASAP), 2013 IEEE 24th International Conference on*, pp. 91-94, June 2013.

[19] J. Fowers and G. Stitt, "Dynafuse: dynamic dependence analysis for FPGA pipeline fusion and locality optimizations," in *Proceedings of the ACM/SIGDA international symposium on Field programmable gate arrays*, FPGA '13, pp. 201–210, February 2013.

[20] A. Landy and G. Stitt, "A low-overhead interconnect architecture for virtual reconfigurable fabrics," in *CASES'12: Proceedings of the 2012 international conference on Compilers, architectures and synthesis for embedded systems*, CASES '12, pp. 111–120, October 2012.

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[22] J. Coole and G. Stitt, "BPR: fast FPGA placement and routing using macroblocks," in *CODES+ISSS'12: Proceedings of the eighth IEEE/ACM/IFIP international conference on Hardware/software codesign and system synthesis*, CODES+ISSS '12, pp. 275–284, October 2012.

[23] J. Curreri, G. Stitt, and A. George, "Communication visualization for bottleneck detection of high-level synthesis applications," in *FPGA '12: Proceedings of the ACM/SIGDA international symposium on Field Programmable Gate Arrays*, FPGA '12, pp. 33–36, February 2012.

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[25] R. Kirchgessner, G. Stitt, A. George, and H. Lam, "VirtualRC: a virtual FPGA platform for applications and tools portability," in *FPGA '12: Proceedings of the ACM/SIGDA international symposium on Field Programmable Gate Arrays*, FPGA '12, pp. 205–208, February 2012.

[26] J. Fowers, G. Brown, P. Cooke, and G. Stitt, "A performance and energy comparison of FPGAs, GPUs, and multicores for sliding-window applications," in *FPGA '12: Proceedings of the ACM/SIGDA international symposium on Field Programmable Gate Arrays*, FPGA '12, pp. 47–56, February 2012.

[27] V. Aggarwal, C. Yoon, A. George, H. Lam, and G. Stitt, "Performance modeling for multilevel communication in shmem+," in *PGAS'10: Proceedings of the Conference on Partitioned Global Address Space Programming Model*, p. 10, October 2010.

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[29] J. Coole and G. Stitt, "Intermediate fabrics: Virtual architectures for circuit portability and fast placement and routing," in *CODES/ISSS '10: Proceedings of the IEEE/ACM/IFIP international conference on Hardware/Software codesign and system synthesis*, pp. 13–22, October 2010.

[30] A. George, H. Lam, C. Pascoe, A. Lawande, and G. Stitt, "Novo-g: A view at the hpc crossroads for scientific computing," in *ERSA'10: Proceedings of the International Conference on Engineering of Reconfigurable Systems and Algorithms*, July 2010.

[31] C. Reardon, A. George, G. Stitt, and H. Lam, "An automated scheduling and partitioning algorithm for scalable rc systems," in *ERSA'10: Proceedings of the International Conference on Engineering of Reconfigurable Systems and Algorithms*, July 2010.

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[34] J. Coole, J. Wernsing, and G. Stitt, "A traversal cache framework for fpga acceleration of pointer data structures: A case study on barnes-hut n-body simulation," in *Reconfigurable Computing and FPGAs, 2009. ReConFig '09. International Conference on*, pp. 143-148, Dec. 2009.

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Technical Reports

[1] G. Stitt and F. Vahid. Binary-level hardware/software partitioning of MediaBench, NetBench, and EEMBC benchmarks. Tech. Rep. UCR-CSE-03-01, University of California, Riverside, January 2003.

Funding

- National Science Foundation. CNS-1718033, CSR: EAGER: Quality-of-Experience-Aware Runtime Optimizations for Heterogeneous Multi-Core Systems, $278,382 July 2017-June 2019, PI: Ann Gordon-Ross, Co-PI: **G. Stitt**
- NSF Center for Space, High-Performance, and Resilient Computing (SHREC) *FPGA Virtualization & Application Case Studies*, $120,000, January 2018-December 2018, PI: **G. Stitt**, Co-PI: A. Gordon-Ross
- NSF Center for High-Performance Reconfigurable Computing (CHREC) *FPGA Virtualization & Application Case Studies*, $120,000, January 2017-December 2017, PI: **G. Stitt**, Co-PI: A. Gordon-Ross
- Harris Endowed Seed Fund. *Thermal Aware Computing: Hardware Monitoring and Software Controls*, $40,000, January 2016-December 2018, PI: **G. Stitt**, Co-PI: S. Ranka
- NSF Center for High-Performance Reconfigurable Computing (CHREC), *Virtualization-Enabled FPGA Optimizations*, $152,000, January 2016-December 2016, PI: **G. Stitt**, Co-PI: A. Gordon-Ross
- NSF Center for High-Performance Reconfigurable Computing (CHREC), *VAPoR – Virtualization for Adaptivity, Productivity, Portability, and Redundancy*, $120,000, January 2015-December 2015, PI: **G. Stitt**, Co-PI: A. Gordon-Ross
- NSF Center for High-Performance Reconfigurable Computing (CHREC), *FPGA and Many-Core Computing for Aerospace and Defense*, $172,000, January 2015-December 2015, PI: A. George, Co-PI: H. Lam, **G. Stitt**
- DOE/NNSA, *Novo-G Exascale Emulation (NGEE) program, PSAAP-II Center for Compressible Multiphase Turbulence*, $10M (total), $2.214M (NGEE portion), December 2013-January 2019, PI: A. George, Co-PI: H. Lam and **G. Stitt**
- NSF Center for High-Performance Reconfigurable Computing (CHREC), *High-Productivity Design Automation for FPGA Applications*, $80,000, January 2014-December 2014, PI: **G. Stitt**
- NSF Center for High-Performance Reconfigurable Computing (CHREC), *Advanced Computing for Aerospace and Defense*, $158,000, January 2014-December 2014, PI: A. George, Co-PI: H. Lam, **G. Stitt**
- NSF Center for High-Performance Reconfigurable Computing (CHREC), *Virtualization Strategies for Fast FPGA Compilation*, $76,000, January 2013-December 2013, PI: **G. Stitt**
- NSF Center for High-Performance Reconfigurable Computing (CHREC), *Reconfigurable & Many-core Computing for Aerospace & Defense*, $208,000, January 2013-December 2013, PI: A. George, Co-PI: H. Lam, **G. Stitt**
- **National Science Foundation CAREER Award**, CNS-1149285, *Design Virtualization for Mainstream Programming of Reconfigurable Computers*, $450,000, February 2012-January 2017, PI: **G. Stitt**
- NSF Center for High-Performance Reconfigurable Computing (CHREC), *A Unified Design Stack for Productivity - from Modeling to Middleware*, $161,000, January 2012-December 2012, PI: A. George, Co-PI: H. Lam, **G. Stitt**
- NSF Center for High-Performance Reconfigurable Computing (CHREC), *Rapid Application Design and Compilation for FPGAs*, $66,500, January 2012-December 2012, PI: **G. Stitt**

- NSF Center for High-Performance Reconfigurable Computing (CHREC), *Tools Research for Application Design Productivity*, $173,000, January 2011-December 2011, PI: **G. Stitt**, Co-PI: A. George, H. Lam
- NSF Center for High-Performance Reconfigurable Computing (CHREC), *Applications Research for RC Systems*, $183,000, January 2011-December 2011, PI: H. Lam, Co-PI: A. George, **G. Stitt**
- NSF Center for High-Performance Reconfigurable Computing (CHREC), *Hardware Virtualization Layer for Ubiquitous RC*, $84,000, January 2010-December 2010, PI: **G. Stitt**, Co-PI: A. George
- NSF Center for High-Performance Reconfigurable Computing (CHREC), *Comprehensive Framework for Application Development Productivity*, $118,000, January 2010-December 2010, PI: A. George, Co-PIs: H. Lam and **G. Stitt**
- National Science Foundation, CNS-0914474, *CSR: Small: Elastic Computing - An Enabling Technology for Transparent, Portable, and Adaptive Multi-Core Heterogeneous Computing*, $405,362, August 2009-July 2012, PI: **G. Stitt**
- NSF Center for High-Performance Reconfigurable Computing (CHREC), *Translation and Execution Productivity*, $52,000, January 2009-December 2009, PI: **G. Stitt**, Co-PI: A. George
- NSF Center for High-Performance Reconfigurable Computing (CHREC), *System-Level Formulation and Design*, $140,000, January 2009-December 2009, PI: A. George, Co-PIs: H. Lam and **G. Stitt**

Awards

- University of Florida College of Engineering *Undergraduate Teacher of the Year* (2014-2015 Academic Year)
- **National Science Foundation CAREER Award**, CNS-1149285, *Design Virtualization for Mainstream Programming of Reconfigurable Computers*, $450,000, February 2012-January 2017, PI: **G. Stitt**

Donations

- Altera Corporation, Terasic DE2-70 FPGA Development Board, February 2009, Commercial Value: $599