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Gregory Stitt

Research Interests

Reconfigurable computing: emphasis in design automation, synthesis, compilers, embedded systems, hardware/software co-design, low-power design, system-on-a-chip multi-core architectures, and run-time optimizations.

Approximate Computing: emphasis on program synthesis, symbolic regression, parallelizing approximation discovery.

Education

- Ph.D. Computer Science, University of California, Riverside, June 2007, Thesis title: *Synthesis From Software Binaries: An Enabling Technology for Dynamic and Transparent Synthesis*, Advisor: Dr. Frank Vahid
- B.S. Computer Science, University of California, Riverside, June 2000, GPA: 3.953, Summa Cum Laude

Employment

- Professor, University of Florida, Department of Electrical and Computer Engineering, August 2021 to present
- Associate Professor, University of Florida, Department of Electrical and Computer Engineering, August 2013 to August 2021
- Assistant Professor, University of Florida, Department of Electrical and Computer Engineering, August 2007 to August 2013

Teaching

- EEL6935 (Reconfigurable Computing 2) –Professor, UF (Spring 2022-2023)
- EEL4712 (Digital Design) – Assistant/Associate/Full Professor, UF (Spring 2010-2023)
- EEL5721/EEL4720 (Reconfigurable Computing) – Assistant/Associate/Full Professor, UF (Fall 2012-2023)
- EEL4930/EEL5934 (Reconfigurable Computing) – Assistant Professor, UF (Fall 2007-2011, Spring 2008-2009)
- CS 161L (Computer Architecture) – Lecturer, UCR (Spring 2005)
- CS 161 (Computer Architecture) - Teaching assistant, UCR (Fall 2001)
- CS 122A (Embedded Systems) - Teaching assistant, UCR (Fall 2000, 2003)
- CS 122B (Adv. Embedded Systems) - Teaching assistant, UCR (Winter 2003, 2004)
- Computer science tutor, UCR Learning Center (1999)

Teaching Evaluations

- 2022 Fall: 4.78, 4.76 (5.0 max)
- 2022 Spring: 4.88, 4.69 (5.0 max)
- 2021 Fall: 4.86, 4.71 (5.0 max)
- 2021 Spring: 4.85 (5.0 max)
- 2020 Fall: 4.81, 4.63, 4.71 (5.0 max)
- 2020 Spring: 4.88 (5.0 max)
- 2019 Fall: 4.94, 4.83 (5.0 max)
- 2019 Spring: 4.93 (5.0 max)
- 2018 Fall: 4.96, 5.0 (5.0 max)
- 2018 Spring: 4.82 (5.0 max)
- 2017 Spring: 4.86 (5.0 max)
- 2016 Fall: 4.92, 4.90 (5.0 max)
- 2016 Spring: 4.81 (5.0 max)
- 2015 Fall : 4.88,4.89 (5.0 max)

- 2015 Spring: 4.69 (5.0 max)
- 2014 Fall: 4.82,4.62 (5.0 max)

Patents

[1] G. Stitt, D. Campbell, R. Aloni, T. Vaseliou, J. Salkey. Architecture-Independent Approximation Discovery. Serial No. 62/527,667; filed June 30, 2017. UF#-16791

[2] K. Yang. K. Robert, S. Bhunia, G. Stitt. A Uniquified FPGA Virtualization Approach to Hardward Security, Filed 12/13/2016, UF# 16477

[3] J. Coole and G. Stitt. Overlay Architecture For Programing FPGAs. Filed 4/29/2016, U.S. Provisional App. No.: 62/329,944; UF# 16190

[4] G. Stitt and J. Wernsing. Elastic Computing, filed 04/11/11, UF#-13728, 222106-8135, Patent Application Serial No. 61/474,020.

[5] F. Vahid, R. Lysecky, and G. Stitt. Warp processor for dynamic hardware/software partitioning, 2008, US Patent 7,356,672.

Journal Publications

[1] G. Stitt and D. Campbell, "Pandora: An architecture-independent parallelizing approximation-discovery framework," *ACM Trans. Embed. Comput. Syst.*, vol. 19, November 2020.

[2] G. Stitt, R. Karam, K. Yang, and S. Bhunia, "A uniquified virtualization approach to hardware security," *IEEE Embedded Systems Letters*, vol. 9, pp. 53–56, September 2017.

[3] D. Wilson, A. Shastri, and G. Stitt, "A high-level synthesis scheduling and binding heuristic for fpga fault tolerance," *International Journal of Reconfigurable Computing*, vol. 2017, p. 17, August 2017.

[4] A. Landy and G. Stitt, "Serial arithmetic strategies for improving fpga throughput," *ACM Trans. Embed. Comput. Syst.*, vol. 16, pp. 84:1–84:25, July 2017.

[5] D. Wilson and G. Stitt, "A scalable, low-overhead finite-state machine overlay for rapid FPGA application development," *CoRR*, vol. abs/1705.02732, p. 6, February 2017.

[6] D. Wilson and G. Stitt, "The unified accumulator architecture: A configurable, portable, and extensible floating-point accumulator," *ACM Trans. Reconfigurable Technol. Syst.*, vol. 9, pp. 21:1–21:23, May 2016.

[7] G. Stitt, E. Schwartz, and P. Cooke, "A parallel sliding-window generator for high-performance digital-signal processing on fpgas," *ACM Trans. Reconfigurable Technol. Syst.*, vol. 9, pp. 23:1–23:22, May 2016.

[8] G. Wang, G. Stitt, H. Lam, and A. George, "Core-level modeling and frequency prediction for dsp applications on fpgas," *International Journal of Recconfigurable Computing*, p. 20, September 2015.

[9] R. Kirchgessner, A. D. George, and G. Stitt, "Low-overhead fpga middleware for application portability and productivity," *ACM Trans. Reconfigurable Technol. Syst.*, vol. 8, pp. 21:1–21:22, September 2015.

[10] P. Cooke, L. Hao, and G. Stitt, "Finite-state-machine overlay architectures for fast fpga compilation and application portability," *ACM Trans. Embed. Comput. Syst.*, vol. 14, April 2015.

[11] P. Cooke, J. Fowers, G. Brown, and G. Stitt, "A tradeoff analysis of fpgas, gpus, and multicores for sliding-window applications," *ACM Transactions on Reconfigurable Technology and Systems (TRETS)*, vol. 8, pp. 2:1–2:24, Mar 2015.

[12] J. Coole and G. Stitt, "Fast, flexible high-level synthesis from opencl using reconfiguration contexts," *Micro, IEEE*, vol. 34, pp. 42–53, Jan 2014.

[13] J. Fowers, G. Brown, J. Wernsing, and G. Stitt, "A performance and energy comparison of convolution on GPUs, FPGAs, and multicore processors," *ACM Transactions on Architecture and Code Optimization (TACO) - Special Issue on High-Performance Embedded Architectures and Compilers*, vol. 9, pp. 25:1–25:21, January 2013.

[14] L. Hao and G. Stitt, "Bandwidth-sensitivity-aware arbitration for FPGAs," *Embedded Systems Letters, IEEE*, vol. 4, pp. 73–76, September 2012.

[15] C. Reardon, B. Holland, A. D. George, G. Stitt, and H. Lam, "Rcml: An environment for estimation modeling of reconfigurable computing systems," *ACM Transactions on Embedded Computing Systems (TECS): Special Section on CAPA'09*, vol. 11, pp. 43:1–43:22, August 2012.

[16] J. R. Wernsing and G. Stitt, "Elastic computing: A portable optimization framework for hybrid computers," *Parallel Computing*, vol. 38, pp. 438–464, August 2012.

[17] G. Stitt, "Are field-programmable gate arrays ready for the mainstream? ," *Micro, IEEE*, vol. 31, pp. 58–63, Nov/Dec 2011.

[18] G. Stitt and J. Coole, "Intermediate fabrics: Virtual architectures for near-instant FPGA compilation," *Embedded Systems Letters, IEEE*, vol. 3, pp. 81 –84, sept. 2011.

[19] G. Stitt, A. George, H. Lam, M. Smith, V. Aggarwal, G. Wang, C. Reardon, B. Holland, S. Koehler, and J. Coole, "An end-to-end tool flow for FPGA-accelerated scientific computing," *IEEE Design&Test of Computers: Special Issue on Design Methods and Tools for FPGA-Based Acceleration of Scientific Computing*, vol. 28, pp. 68–77, July/August 2011.

[20] A. George, H. Lam, and G. Stitt, "Novo-g: at the forefront of scalable reconfigurable supercomputing," *IEEE Computing in Science and Engineering Magazine*, pp. 82–86, Jan/Feb 2011.

[21] J. Curreri, G. Stitt, and A. George, "High-level synthesis of in-circuit assertions for verification, debugging, and timing analysis," *International Journal of Reconfigurable Computing*, vol. 2011, pp. 1–17, December 2011.

[22] S. Koehler, G. Stitt, and A. George, "Platform-aware bottleneck detection for reconfigurable computing applications," *ACM Transactions on Reconfigurable Technology and Systems (TRETS)*, vol. 4, pp. 30:1–30:28, August 2011.
[23] V. Aggarwal, G. Stitt, A. George, and C. Yoon, "SCF: A framework for task-level coordination in reconfigurable, heterogeneous systems," *ACM Transactions on Reconfigurable Technology and Systems (TRETS)*, vol. 2011, pp. 1–24, June 2011.
[24] G. Stitt and F. Vahid, "Thread warping: Dynamic and transparent synthesis of thread accelerators," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, vol. 16, pp. 32:1–32:21, June 2011.
[25] J. Coole and G. Stitt, "Traversal caches: A framework for FPGA acceleration of pointer data structures," *International Journal of Reconfigurable Computing*, vol. 2010, pp. 1–16, December 2010.
[26] F. Vahid, G. Stitt, and R. Lysecky, "Warp processing: Dynamic translation of binaries to FPGA circuits," *Computer*, vol. 41, pp. 40–46, July 2008.
[27] G. Stitt and F. Vahid, "Binary synthesis," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, vol. 12, pp. 1–30, August 2007.
[28] R. Lysecky, G. Stitt, and F. Vahid, "Warp processors," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, vol. 11, pp. 659–681, June 2006.
[29] G. Stitt, F. Vahid, and S. Nematbakhsh, "Energy savings and speedups from partitioning critical software loops to hardware in embedded systems," *ACM Transactions on Embedded Computing Systems (TECS)*, vol. 3, pp. 218–232, February 2004.
[30] F. Vahid, R. Lysecky, C. Zhang, and G. Stitt, "Highly configurable platforms for embedded computing systems," *Microelectronics Journal*, vol. 34, pp. 1025 – 1029, November 2003. IEEE Workshop on Embedded System Codesign (ESCODES).
[31] G. Stitt and F. Vahid, "Energy advantages of microprocessor platforms with on-chip configurable logic," *IEEE Design & Test*, vol. 19, pp. 36–43, November 2002.
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[33] F. Vahid, R. Patel, and G. Stitt, "Propagating constants past software to hardware peripherals in fixed-application embedded systems," *ACM SIGARCH Computer Architecture News*, vol. 29, pp. 25–30, December 2001. Selected for special issue from earlier version of paper in Compilers and Operating Systems for Low Power (COLP'01).

Book Chapters

[1] F. Vahid and G. Stitt. *Reconfigurable Computing: The Theory and Practice of FPGA-Based Computation*. Morgan Kaufmann, 2007, ch. (26) Hardware/Software Partitioning, pp. 539–560.
[2] G. Stitt and F. Vahid. *Compilers and operating systems for low power*. Kluwer Academic Publishers, 2003, ch. Propagating Constants Past Software to Hardware Peripherals in Fixed-Application Embedded Systems, pp. 115–135.

Conference Publications

[1] J. Fugate, G. Stitt, N. V. R. Masna, A. Dasgupta, S. Bhunia, N. Dorairaj, and D. Kehlet, "An exploration of atpg methods for redacted ip and reconfigurable hardware," in *IEEE VLSI Test Symposium (VTS)*, April 2023.
[2] C. Crary, W. Piard, G. Stitt, C. Bean, and B. Hicks, "Using FPGA devices to accelerate tree-based genetic programming: A preliminary exploration with recent technologies," in *EuroGP 2023: Proceedings of the 26th European Conference on Genetic Programming* (G. Pappa, M. Giacobini, and Z. Vasicek, eds.), vol. 13986 of *LNCS*, (Brno, Czech Republic), Springer Verlag, April 2023.
[3] J. Fugate, G. Stitt, N. V. R. Masna, A. Dasgupta, S. Bhunia, N. Dorairaj, and D. Kehlet, "Atpg and test methods for redacted ip," in *GOMACTech*, March 2023.
[4] C. Crary, W. Piard, B. Chesley, and G. Stitt, "Work-in-progress: Toward a robust, reconfigurable hardware accelerator for tree-based genetic programming," in *2022 International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)*, pp. 17–18, October 2022.
[5] S. P. Chenna, H. Lam, G. Stitt, and S. Balachandar, "Scalable performance prediction of irregular workloads in multi-phase particle-in-cell applications," in *2021 IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW)*, pp. 816–825, 2021.
[6] R. Blanchard, G. Stitt, and H. Lam, "Fpga acceleration of fluid-flow kernels," in *2020 IEEE/ACM International Workshop on Heterogeneous High-performance Reconfigurable Computing (H2RC)*, pp. 29–37, 2020.
[7] D. Wilson and G. Stitt, "Seiba: An fpga overlay-based approach to rapid application development," in *International Conference on Reconfigurable Computing and FPGAs*, pp. 1–8, Dec 2019.
[8] R. Vazquez, A. Gordon-Ross, and G. Stitt, "Energy prediction for cache tuning in embedded systems," in *2019 IEEE International Conference on Computer Design (ICCD)*, pp. 1–8, Nov 2019.
[9] R. Vazquez, A. Gordon-Ross, and G. Stitt, "Work-in-progress: Offloading cache configuration prediction to an fpga for hardware speedup and overhead reduction," in *2019 International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, pp. 1–2, Oct 2019.
[10] R. Vazquez, A. Gordon-Ross, and G. Stitt, "Machine learning-based prediction for dynamic architectural optimizations," in *2019 Tenth International Green and Sustainable Computing Conference (IGSC)*, pp. 1–6, Oct 2019.
[11] R. Vazquez, A. Gordon-Ross, and G. Stitt, "Machine learning-based prediction for dynamic, runtime architectural optimizations of embedded systems," in *2019 IEEE Nordic Circuits and Systems Conference (NORCAS): NORCHIP and International Symposium*

of System-on-Chip (SoC), pp. 1–7, Oct 2019.
[12] C. Pascoe, R. Blanchard, H. Lam, and G. Stitt, "A fpga-pipelined, high-throughput approach to coarse-grained simulation of hpc systems," in *International Workshop on Modeling and Simulation of and by Parallel and Distributed Systems (MSPDS*, p. 10, July 2019.
[13] S. Chenna, G. Stitt, and H. Lam, "Multi-parameter performance modeling using symbolic regression," in *International Conference on High Performance Computing & Simulation (HPCS)*, p. 10, July 2019.
[14] G. Stitt and D. Campbell, "Pandora: A parallelizing approximation-discovery framework (wip paper)," in *Proceedings of the 20th ACM SIGPLAN/SIGBED International Conference on Languages, Compilers, and Tools for Embedded Systems*, LCTES 2019, (New York, NY, USA), p. 198–202, Association for Computing Machinery, June 2019.
[15] A. Edun, R. Vazquez, A. Gordon-Ross, and G. Stitt, "Dynamic scheduling on heterogeneous multicores," in *2019 Design, Automation Test in Europe Conference Exhibition (DATE)*, pp. 1685–1690, March 2019.
[16] A. Ramaswamy, N. Kumar, A. Neelakantan, H. Lam, and G. Stitt, "Scalable behavioral emulation of extreme-scale systems using structural simulation toolkit," in *Proceedings of the 47th International Conference on Parallel Processing*, ICPP 2018, (New York, NY, USA), pp. 17:1–17:11, ACM, August 2018.
[17] D. Wilson, G. Stitt, and J. Coole, "A recurrently generated overlay architecture for rapid fpga application development," in *Proceedings of the 9th International Symposium on Highly-Efficient Accelerators and Reconfigurable Technologies*, HEART 2018, (New York, NY, USA), pp. 4:1–4:6, ACM, June 2018.
[18] M. N. Emas, A. Baylis, and G. Stitt, "High-frequency absorption-fifo pipelining for stratix 10 hyperflex," in *2018 IEEE 26th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, pp. 97–100, April 2018.
[19] G. Stitt, A. Gupta, M. N. Emas, D. Wilson, and A. Baylis, "Scalable window generation for the intel broadwell+arria 10 and high-bandwidth fpga systems," in *Proceedings of the 2018 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays*, FPGA '18, (New York, NY, USA), pp. 173–182, ACM, February 2018.
[20] C. Pascoe, S. Chenna, G. Stitt, and H. Lam, "A fpga-pipelined approach for accelerated discrete-event simulation of hpc systems," in *Heterogeneous High-performance Reconfigurable Computing (H2RC)*, p. 2, November 2017.
[21] A. Baylis, G. Stitt, and A. Gordon-Ross, "Overlay-based side-channel countermeasures: A case study on correlated noise generation," in *2017 IEEE 60th International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 1308–1311, August 2017.
[22] D. Wilson and G. Stitt, "A scalable, low-overhead finite-state machine overlay for rapid fpga application development," in *International Workshop on Overlay Architectures for FPGAs (OLAF), co-located with FPGA 2017*, p. 6, February 2017.
[23] N. Kumar, C. Pascoe, C. Hajas, H. Lam, G. Stitt, and A. George, "Behavioral emulation for scalable design-space exploration of algorithms and architectures," in *International Conference on High Performance Computing*, pp. 5–17, 2016.
[24] C. Pascoe, N. Kumar, H. Lam, and G. Stitt, "Fpga-pipelined discrete-event simulations for accelerated behavioral emulation of extreme-scale systems," in *Workshop on Modeling & Simulation of Systems & Applications (ModSim)*, p. 2, 2016.
[25] N. Kumar, A. George, H. Lam, G. Stitt, and S. Hammond, "Understanding performance and reliability trade-offs for extreme-scale systems using behavioral emulation," in *Workshop on Modeling & Simulation of Systems and Applications (ModSim)*, 2015.
[26] A. Shastri, G. Stitt, and E. Riccio, "A scheduling and binding heuristic for high-level synthesis of fault-tolerant fpga applications," in *Application-specific Systems, Architectures and Processors (ASAP), 2015 IEEE 26th International Conference on*, pp. 202–209, July 2015.
[27] D. Rudolph and G. Stitt, "An interpolation-based approach to multi-parameter performance modeling for heterogeneous systems," in *Application-specific Systems, Architectures and Processors (ASAP), 2015 IEEE 26th International Conference on*, pp. 174–180, July 2015.
[28] A. Landy and G. Stitt, "Revisiting serial arithmetic: A performance and tradeoff analysis for parallel applications on modern fpgas," in *Field-Programmable Custom Computing Machines (FCCM), 2015 IEEE 23rd Annual International Symposium on*, pp. 9–16, May 2015.
[29] J. Coole and G. Stitt, "Adjustable-cost overlays for runtime compilation," in *Field-Programmable Custom Computing Machines (FCCM), 2015 IEEE 23rd Annual International Symposium on*, pp. 21–24, May 2015.
[30] J. Fowers, J. Liu, and G. Stitt, "A framework for dynamic parallelization of fpga-accelerated applications," in *Proceedings of the 17th International Workshop on Software and Compilers for Embedded Systems*, SCOPES '14, (New York, NY, USA), pp. 1–10, ACM, June 2014.
[31] J. Fowers, K. Ovtcharov, K. Strauss, E. S. Chung, and G. Stitt, "A high memory bandwidth fpga accelerator for sparse matrix-vector multiplication," in *Proceedings of the 2014 IEEE 22nd International Symposium on Field-Programmable Custom Computing Machines*, FCCM '14, (Washington, DC, USA), pp. 36–43, IEEE Computer Society, May 2014.
[32] J. Coole and G. Stitt, "Opencl high-level synthesis for mainstream fpga acceleration," in *Workshop on SoCs, Heterogeneous Architectures and Workloads (SHAW)*, feb 2014.
[33] P. Cooke, J. Fowers, G. Stitt, and L. Hunt, "A comparison of correntropy-based feature tracking on fpgas and gpus," in *Application-Specific Systems, Architectures and Processors (ASAP), 2013 IEEE 24th International Conference on*, pp. 237–240, June 2013.
[34] L. Hao and G. Stitt, "Virtual finite-state-machine architectures for fast compilation and portability," in *Application-Specific Systems, Architectures and Processors (ASAP), 2013 IEEE 24th International Conference on*, pp. 91–94, June 2013.
[35] A. Landy and G. Stitt, "Pseudo-constant logic optimization," in *Application-Specific Systems, Architectures and Processors (ASAP), 2013 IEEE 24th International Conference on*, pp. 99–102, June 2013.
[36] J. Fowers and G. Stitt, "Dynafuse: dynamic dependence analysis for FPGA pipeline fusion and locality optimizations," in

Proceedings of the ACM/SIGDA international symposium on Field programmable gate arrays, FPGA '13, (New York, NY, USA), pp. 201–210, ACM, February 2013.

[37] A. Landy and G. Stitt, "A low-overhead interconnect architecture for virtual reconfigurable fabrics," in *CASES'12: Proceedings of the 2012 international conference on Compilers, architectures and synthesis for embedded systems*, CASES '12, (New York, NY, USA), pp. 111–120, ACM, October 2012.

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[39] J. Coole and G. Stitt, "BPR: fast FPGA placement and routing using macroblocks," in *CODES+ISSS'12: Proceedings of the eighth IEEE/ACM/IFIP international conference on Hardware/software codesign and system synthesis*, CODES+ISSS '12, (New York, NY, USA), pp. 275–284, ACM, October 2012.

[40] J. Fowers, G. Brown, P. Cooke, and G. Stitt, "A performance and energy comparison of FPGAs, GPUs, and multicores for sliding-window applications," in *FPGA '12: Proceedings of the ACM/SIGDA international symposium on Field Programmable Gate Arrays*, FPGA '12, (New York, NY, USA), pp. 47–56, ACM, February 2012.

[41] R. Kirchgessner, G. Stitt, A. George, and H. Lam, "VirtualRC: a virtual FPGA platform for applications and tools portability," in *FPGA '12: Proceedings of the ACM/SIGDA international symposium on Field Programmable Gate Arrays*, FPGA '12, (New York, NY, USA), pp. 205–208, ACM, February 2012.

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[43] J. Curreri, G. Stitt, and A. George, "Communication visualization for bottleneck detection of high-level synthesis applications," in *FPGA '12: Proceedings of the ACM/SIGDA international symposium on Field Programmable Gate Arrays*, FPGA '12, (New York, NY, USA), pp. 33–36, ACM, February 2012.

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[47] A. George, H. Lam, C. Pascoe, A. Lawande, and G. Stitt, "Novo-g: A view at the hpc crossroads for scientific computing," in *ERSA'10: Proceedings of the International Conference on Engineering of Reconfigurable Systems and Algorithms*, July 2010.

[48] C. Reardon, A. George, G. Stitt, and H. Lam, "An automated scheduling and partitioning algorithm for scalable rc systems," in *ERSA'10: Proceedings of the International Conference on Engineering of Reconfigurable Systems and Algorithms*, July 2010.

[49] J. Curreri, G. Stitt, and A. George, "High-level synthesis techniques for in-circuit assertion-based verification," in *RAW '10: Proceedings of the 17th Reconfigurable Architectures Workshop*, April 2010.

[50] J. Wernsing and G. Stitt, "Elastic computing: A framework for transparent, portable, and adaptive multi-core heterogeneous computing," in *LCTES '10: Proceedings of the 2010 ACM SIGPLAN/SIGBED conference on Languages, compilers, and tools for embedded systems*, pp. 115–124, ACM, April 2010.

[51] J. Coole, J. Wernsing, and G. Stitt, "A traversal cache framework for fpga acceleration of pointer data structures: A case study on barnes-hut n-body simulation," in *Reconfigurable Computing and FPGAs, 2009. ReConFig '09. International Conference on*, pp. 143–148, Dec. 2009.

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[53] V. Aggarwal, R. Garcia, G. Stitt, A. George, and H. Lam, "Scf: a device- and language-independent task coordination framework for reconfigurable, heterogeneous systems," in *HPRCTA '09: Proceedings of the Third International Workshop on High-Performance Reconfigurable Computing Technology and Applications*, (New York, NY, USA), pp. 19–28, ACM, November 2009.

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[55] G. Stitt, G. Chaudhari, and J. Coole, "Traversal caches: a first step towards FPGA acceleration of pointer-based data structures," in *CODES/ISSS '08: Proceedings of the 6th IEEE/ACM/IFIP international conference on Hardware/Software codesign and system synthesis*, (New York, NY, USA), pp. 61–66, ACM, October 2008.

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[57] S. Merchant, B. Holland, C. Reardon, A. George, H. Lam, G. Stitt, M. Smith, N. Alam, I. Gonzalez, E. El-Araby, P. Saha, T. El-Ghazawi, and H. Simmler, "Strategic challenges for application development productivity in reconfigurable computing," in *IEEE National Aerospace and Electronics Conference (NAECON)*, July 2008.

[58] G. Stitt, "Hardware/software partitioning with multi-version implementation exploration," in *GLSVLSI '08: Proceedings of the 18th ACM Great Lakes symposium on VLSI*, (New York, NY, USA), pp. 143–146, ACM, May 2008.

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Technical Reports

[1] G. Stitt and F. Vahid. Binary-level hardware/software partitioning of MediaBench, NetBench, and EEMBC benchmarks. Tech. Rep. UCR-CSE-03-01, University of California, Riverside, January 2003.

Funding

- Intel. *Intel Gift Funds for SYCL Course Development*. $50,000, May 2022-April 2023. PI: **G.Stitt**
- National Science Foundation. 2114165. *Collaborative Research: SaTC: EDU: Hardware Security Education for All Through Seamless Extension of Existing Curricula*. $89,999 ($20,100 Co-PI). PI: Swarup Bhunia, Co-PI: **G. Stitt**
- Intel. *Chiplet IP Protection and Countermeasures for State-of-the-art Heterogeneous Integrated Packaging (SHIP) Prototype Project*. $3,160,000 ($500,000 Co-PI). PI: Swarup Bhunia, Co-PI: **G. Stitt.**
- National Science Foundation. CNS-1718033, *SHF: Small: Enabling New Machine-Learning Usage Scenarios with Software-Defined Hardware for Symbolic Regression*, $499,519 October 2019-September 2022, PI: **G. Stitt,** Co-PI: Ann Gordon-Ross
- NSF Center for Space, High-Performance, and Resilient Computing (SHREC) *Tools and App Studies for Heterogeneous Computing*, $120,000, January 2020-December 2020, PI: **G. Stitt**, Co-PIs: H. Lam, A. Gordon-Ross
- Intel. *Intel Gift Funds for ModelSim and Timing Analysis Training Course Development*. $15,000, December 2019-June 2020. PI: **G.Stitt**
- Intel. *Intel Gift Funds for FPGA DevCloud Training Course Development*. $15,000, December 2019-June 2020. PI: **G.Stitt**
- L3Harris. FPGA Virtualization. $40,000, August 2019 to December 2019, PI: **G.Stitt**

- NSF Center for Space, High-Performance, and Resilient Computing (SHREC) *FPGA Virtualization for High-Performance and Secure Application Design*, $120,000, January 2019-December 2019, PI: **G. Stitt**, Co-PI: A. Gordon-Ross
- National Science Foundation. CNS-1718033, CSR: EAGER: Quality-of-Experience-Aware Runtime Optimizations for Heterogeneous Multi-Core Systems, $278,382 July 2017-June 2019, PI: Ann Gordon-Ross, Co-PI: **G. Stitt ($135,882)**
- NSF Center for Space, High-Performance, and Resilient Computing (SHREC) *FPGA Virtualization & Application Case Studies*, $120,000, January 2018-December 2018, PI: **G. Stitt**, Co-PI: A. Gordon-Ross
- NSF Center for High-Performance Reconfigurable Computing (CHREC) *FPGA Virtualization & Application Case Studies*, $120,000, January 2017-December 2017, PI: **G. Stitt**, Co-PI: A. Gordon-Ross
- Harris Endowed Seed Fund. *Thermal Aware Computing: Hardware Monitoring and Software Controls*, $40,000, January 2016-December 2018, PI: **G. Stitt**, Co-PI: S. Ranka
- NSF Center for High-Performance Reconfigurable Computing (CHREC), *Virtualization-Enabled FPGA Optimizations*, $152,000, January 2016-December 2016, PI: **G. Stitt**, Co-PI: A. Gordon-Ross
- NSF Center for High-Performance Reconfigurable Computing (CHREC), *VAPoR – Virtualization for Adaptivity, Productivity, Portability, and Redundancy*, $120,000, January 2015-December 2015, PI: **G. Stitt**, Co-PI: A. Gordon-Ross
- NSF Center for High-Performance Reconfigurable Computing (CHREC), *FPGA and Many-Core Computing for Aerospace and Defense*, $172,000, January 2015-December 2015, PI: A. George, Co-PI: H. Lam, **G. Stitt**
- DOE/NNSA, *Novo-G Exascale Emulation (NGEE) program, PSAAP-II Center for Compressible Multiphase Turbulence*, $10M (total), $2.214M (NGEE portion), December 2013-January 2019, PI: A. George, Co-PI: H. Lam and **G. Stitt**
- NSF Center for High-Performance Reconfigurable Computing (CHREC), *High-Productivity Design Automation for FPGA Applications*, $80,000, January 2014-December 2014, PI: **G. Stitt**
- NSF Center for High-Performance Reconfigurable Computing (CHREC), *Advanced Computing for Aerospace and Defense*, $158,000, January 2014-December 2014, PI: A. George, Co-PI: H. Lam, **G. Stitt**
- NSF Center for High-Performance Reconfigurable Computing (CHREC), *Virtualization Strategies for Fast FPGA Compilation*, $76,000, January 2013-December 2013, PI: **G. Stitt**
- NSF Center for High-Performance Reconfigurable Computing (CHREC), *Reconfigurable & Many-core Computing for Aerospace & Defense*, $208,000, January 2013-December 2013, PI: A. George, Co-PI: H. Lam, **G. Stitt**
- **National Science Foundation CAREER Award**, CNS-1149285, *Design Virtualization for Mainstream Programming of Reconfigurable Computers*, $450,000, February 2012-January 2017, PI: **G. Stitt**
- NSF Center for High-Performance Reconfigurable Computing (CHREC), *A Unified Design Stack for Productivity - from Modeling to Middleware*, $161,000, January 2012-December 2012, PI: A. George, Co-PI: H. Lam, **G. Stitt**
- NSF Center for High-Performance Reconfigurable Computing (CHREC), *Rapid Application Design and Compilation for FPGAs*, $66,500, January 2012-December 2012, PI: **G. Stitt**
- NSF Center for High-Performance Reconfigurable Computing (CHREC), *Tools Research for Application Design Productivity*, $173,000, January 2011-December 2011, PI: **G. Stitt**, Co-PI: A. George, H. Lam
- NSF Center for High-Performance Reconfigurable Computing (CHREC), *Applications Research for RC Systems*, $183,000, January 2011-December 2011, PI: H. Lam, Co-PI: A. George, **G. Stitt**
- NSF Center for High-Performance Reconfigurable Computing (CHREC), *Hardware Virtualization Layer for Ubiquitous RC*, $84,000, January 2010-December 2010, PI: **G. Stitt**, Co-PI: A. George
- NSF Center for High-Performance Reconfigurable Computing (CHREC), *Comprehensive Framework for Application Development Productivity*, $118,000, January 2010-December 2010, PI: A. George, Co-PIs: H. Lam and **G. Stitt**
- National Science Foundation, CNS-0914474, *CSR: Small: Elastic Computing - An Enabling Technology for Transparent, Portable, and Adaptive Multi-Core Heterogeneous Computing*, $405,362, August 2009-July 2012, PI: **G. Stitt**
- NSF Center for High-Performance Reconfigurable Computing (CHREC), *Translation and Execution Productivity*, $52,000, January 2009-December 2009, PI: **G. Stitt**, Co-PI: A. George
- NSF Center for High-Performance Reconfigurable Computing (CHREC), *System-Level Formulation and Design*, $140,000, January 2009-December 2009, PI: A. George, Co-PIs: H. Lam and **G. Stitt**

Professional Service

- Associate Editor: IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. 2016-2018
- Program Committees:
  - ACM/EDAC/IEEE Design Automation Conference (DAC) (2016-2017)
  - IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM) (2010-2023)
  - International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS) (2011-2023)

- IEEE International Conference on Application-Specific Systems, Architectures, and Processors (ASAP) (2014-2018)
- International Conference on Reconfigurable Computing and FPGAs (Reconfig) (2013-2019)
- International Conference on Languages Compilers, Tools and Theory of Embedded Systems (LCTES) (2014, 2019)
- IEEE Computer Society Annual Symposium on VLSI (ISVLSI) (2009)
- International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES) (2009)

❖ Reviewer: ACM Transactions on Design Automation and Electronic Systems (TODAES), ACM Transactions on Embedded Computing Systems (TECS), IEEE Embedded Systems Letters (ESL), IEEE Transactions on VLSI Systems (TVLSI), Journal of Computer Science and Technology (JCST), IEEE Transactions on Computers (TC), ACM/EDAC/IEEE Design Automation Conference (DAC), IEEE Micro, IEEE Transactions on Parallel and Distributed Systems (TPDS), ACM Computing Surveys International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES), Design Automation for Embedded Systems (DAES), Journal of Parallel and Distributed Computing (JPDC), International Journal of Reconfigurable Computing (IJRC), Design Automation for Embedded Systems (DAEM), Journal of Signal Processing Systems (JSPS), Computers and Electrical Engineering.

Awards

❖ Ruth and Joel Spira Excellence in Teaching Award. May 2021

❖ University of Florida College of Engineering *Undergraduate Teacher of the Year* (2019-2020 Academic Year)

❖ **Best Paper Award.** D. Wilson, G. Stitt, and J. Coole, "A recurrently generated overlay architecture for rapid fpga application development," in *Proceedings of the 9th International Symposium on Highly-Efficient Accelerators and Reconfigurable Technologies*, HEART 2018, (New York, NY, USA), pp. 4:1–4:6, ACM, 2018.

❖ HKN Faculty Member of the Year Award 2016-2017

❖ University of Florida College of Engineering *Undergraduate Teacher of the Year* (2014-2015 Academic Year)

❖ IEEE/HKN Professor of the Year 2013-2014

❖ Pramod P. Khargonekar Junior Faculty Award for Excellence. 2013

❖ **National Science Foundation CAREER Award**, CNS-1149285, *Design Virtualization for Mainstream Programming of Reconfigurable Computers*, $450,000, February 2012-January 2017, PI: **G. Stitt**

Donations

❖ Intel, Stratix 10 GX Signal Integrity Development Kit, September 2018, Commercial Value: $11,000, 3 boards

❖ Altera Corporation, Terasic DE2-70 FPGA Development Board, February 2009, Commercial Value: $599