

Gregory Stitt

Research Interests

Reconfigurable computing: emphasis in design automation, synthesis, compilers, embedded systems, hardware/software co-design, low power-design, system-on-a-chip multi-core architectures, and run-time optimizations.

Education

- ❖ Ph.D. Computer Science, University of California, Riverside, June 2007, Thesis title: *Synthesis From Software Binaries: An Enabling Technology for Dynamic and Transparent Synthesis*, Advisor: Dr. Frank Vahid
- ❖ B.S. Computer Science, University of California, Riverside, June 2000, GPA: 3.953, Summa Cum Laude

Employment

- ❖ Associate Professor, University of Florida, Department of Electrical and Computer Engineering, August 2013 to current
- ❖ Assistant Professor, University of Florida, Department of Electrical and Computer Engineering, August 2007 to August 2013

Teaching

- ❖ EEL4712 (Digital Design) – Assistant/Associate Professor, UF (Spring 2010-2017)
- ❖ EEL5721/EEL4720 (Reconfigurable Computing) – Assistant/Associate Professor, UF (Fall 2012-2016)
- ❖ EEL4930/EEL5934 (Reconfigurable Computing) – Assistant Professor, UF (Fall 2007-2011, Spring 2008-2009)
- ❖ CS 161L (Computer Architecture) – Lecturer, UCR (Spring 2005)
- ❖ CS 161 (Computer Architecture) - Teaching assistant, UCR (Fall 2001)
- ❖ CS 122A (Embedded Systems) - Teaching assistant, UCR (Fall 2000, 2003)
- ❖ CS 122B (Adv. Embedded Systems) - Teaching assistant, UCR (Winter 2003, 2004)
- ❖ Computer science tutor, UCR Learning Center (1999)

Patents

- [1] K. Yang, K. Robert, S. Bhunia, G. Stitt. A Uniquified FPGA Virtualization Approach to Hardware Security, Filed 12/13/2016, UF# 16477
- [2] J. Coole and G. Stitt. Overlay Architecture For Programing FPGAs. Filed 4/29/2016, U.S. Provisional App. No.: 62/329,944; UF# 16190
- [3] G. Stitt and J. Wernsing. Elastic Computing, filed 04/11/11, UF#-13728, 222106-8135, Patent Application Serial No. 61/474,020.
- [4] F. Vahid, R. Lysecky, and G. Stitt. Warp processor for dynamic hardware/software partitioning, 2008, US Patent 7,356,672.

Journal Publications

- [1] G. Stitt, R. Karam, K. Yang, and S. Bhunia, "A uniquified virtualization approach to hardware security," *IEEE Embedded Systems Letters*, vol. PP, no. 99, pp. 1–1, 2017.
- [2] D. Wilson and G. Stitt, "The unified accumulator architecture: A configurable, portable, and extensible floating-point accumulator," *ACM Trans. Reconfigurable Technol. Syst.*, vol. 9, pp. 21:1–21:23, May 2016.
- [3] A. Landy and G. Stitt, "Serial arithmetic strategies for improving fpga throughput," *ACM Transactions on Embedded Computing Systems (TECS)*, to appear.
- [4] G. Stitt, E. Schwartz, and P. Cooke, "A parallel sliding-window generator for high-performance digital-signal processing on fpgas," *ACM Trans. Reconfigurable Technol. Syst.*, vol. 9, pp. 23:1–23:22, May 2016.
- [5] G. Wang, G. Stitt, H. Lam, and A. George, "Core-level modeling and frequency prediction for dsp applications on fpgas," *International Journal of Rec.*, p. 20, 2015.
- [6] R. Kirchgessner, A. D. George, and G. Stitt, "Low-overhead fpga middleware for application portability and productivity," *ACM Trans. Reconfigurable Technol. Syst.*, vol. 8, pp. 21:1–21:22, September 2015.

- [7] P. Cooke, J. Fowers, G. Brown, and G. Stitt, "A tradeoff analysis of fpgas, gpus, and multicores for sliding-window applications," *ACM Transactions on Reconfigurable Technology and Systems (TRET)*, vol. 8, pp. 2:1–2:24, Mar 2015.
- [8] P. Cooke, L. Hao, and G. Stitt, "Finite-state-machine overlay architectures for fast fpga compilation and application portability," *ACM Transactions on Embedded Computing Systems (TECS)*, vol. 1, p. 25, 2014.
- [9] J. Coole and G. Stitt, "Fast, flexible high-level synthesis from opencl using reconfiguration contexts," *Micro, IEEE*, vol. 34, pp. 42–53, Jan 2014.
- [10] J. Fowers, G. Brown, J. Wernsing, and G. Stitt, "A performance and energy comparison of convolution on GPUs, FPGAs, and multicore processors," *ACM Transactions on Architecture and Code Optimization (TACO) - Special Issue on High-Performance Embedded Architectures and Compilers*, vol. 9, pp. 25:1–25:21, January 2013.
- [11] L. Hao and G. Stitt, "Bandwidth-sensitivity-aware arbitration for FPGAs," *Embedded Systems Letters, IEEE*, vol. 4, pp. 73–76, September 2012.
- [12] C. Reardon, B. Holland, A. D. George, G. Stitt, and H. Lam, "Rcml: An environment for estimation modeling of reconfigurable computing systems," *ACM Transactions on Embedded Computing Systems (TECS): Special Section on CAPA'09*, vol. 11, pp. 43:1–43:22, August 2012.
- [13] J. R. Wernsing and G. Stitt, "Elastic computing: A portable optimization framework for hybrid computers," *Parallel Computing*, vol. 38, pp. 438–464, August 2012.
- [14] G. Stitt and J. Coole, "Intermediate fabrics: Virtual architectures for near-instant FPGA compilation," *Embedded Systems Letters, IEEE*, vol. 3, pp. 81–84, sept. 2011.
- [15] G. Stitt, A. George, H. Lam, M. Smith, V. Aggarwal, G. Wang, C. Reardon, B. Holland, S. Koehler, and J. Coole, "An end-to-end tool flow for FPGA-accelerated scientific computing," *IEEE Design&Test of Computers: Special Issue on Design Methods and Tools for FPGA-Based Acceleration of Scientific Computing*, vol. 28, pp. 68–77, July/August 2011.
- [16] G. Stitt, "Are field-programmable gate arrays ready for the mainstream?," *Micro, IEEE*, vol. 31, pp. 58–63, Nov/Dec 2011.
- [17] A. George, H. Lam, and G. Stitt, "Novo-g: at the forefront of scalable reconfigurable supercomputing," *IEEE Computing in Science and Engineering Magazine*, pp. 82–86, Jan/Feb 2011.
- [18] J. Curreri, G. Stitt, and A. George, "High-level synthesis of in-circuit assertions for verification, debugging, and timing analysis," *International Journal of Reconfigurable Computing*, vol. 2011, pp. 1–17, December 2011.
- [19] S. Koehler, G. Stitt, and A. George, "Platform-aware bottleneck detection for reconfigurable computing applications," *ACM Transactions on Reconfigurable Technology and Systems (TRET)*, vol. 4, pp. 30:1–30:28, August 2011.
- [20] V. Aggarwal, G. Stitt, A. George, and C. Yoon, "SCF: A framework for task-level coordination in reconfigurable, heterogeneous systems," *ACM Transactions on Reconfigurable Technology and Systems (TRET)*, vol. 2011, pp. 1–24, June 2011.
- [21] G. Stitt and F. Vahid, "Thread warping: Dynamic and transparent synthesis of thread accelerators," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, vol. 16, pp. 32:1–32:21, June 2011.
- [22] J. Coole and G. Stitt, "Traversal caches: A framework for FPGA acceleration of pointer data structures," *International Journal of Reconfigurable Computing*, vol. 2010, pp. 1–16, December 2010.
- [23] F. Vahid, G. Stitt, and R. Lysecky, "Warp processing: Dynamic translation of binaries to FPGA circuits," *Computer*, vol. 41, pp. 40–46, July 2008.
- [24] G. Stitt and F. Vahid, "Binary synthesis," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, vol. 12, pp. 1–30, August 2007.
- [25] R. Lysecky, G. Stitt, and F. Vahid, "Warp processors," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, vol. 11, pp. 659–681, June 2006.
- [26] G. Stitt, F. Vahid, and S. Nematbakhsh, "Energy savings and speedups from partitioning critical software loops to hardware in embedded systems," *ACM Transactions on Embedded Computing Systems (TECS)*, vol. 3, pp. 218–232, February 2004.
- [27] F. Vahid, R. Lysecky, C. Zhang, and G. Stitt, "Highly configurable platforms for embedded computing systems," *Microelectronics Journal*, vol. 34, pp. 1025–1029, November 2003. IEEE Workshop on Embedded System Codesign (ESCODES).
- [28] J. Villarreal, D. Suresh, G. Stitt, F. Vahid, and W. Najjar, "Improving software performance with configurable logic," *Kluwer Journal on Design Automation of Embedded Systems*, vol. 7, pp. 325–339, November 2002.
- [29] G. Stitt and F. Vahid, "Energy advantages of microprocessor platforms with on-chip configurable logic," *IEEE Design & Test*, vol. 19, pp. 36–43, November 2002.
- [30] F. Vahid, R. Patel, and G. Stitt, "Propagating constants past software to hardware peripherals in fixed-application embedded systems," *ACM SIGARCH Computer Architecture News*, vol. 29, pp. 25–30, December 2001. Selected for special issue from earlier version of paper in Compilers and Operating Systems for Low Power (COLP'01).

Book Chapters

- [1] F. Vahid and G. Stitt. *Reconfigurable Computing: The Theory and Practice of FPGA-Based Computation*. Morgan Kaufmann, 2007, ch. (26) Hardware/Software Partitioning, pp. 539–560.
- [2] G. Stitt and F. Vahid. *Compilers and operating systems for low power*. Kluwer Academic Publishers, 2003, ch. Propagating Constants Past Software to Hardware Peripherals in Fixed-Application Embedded Systems, pp. 115–135.

Conference Publications

- [1] D. Wilson and G. Stitt, "A scalable, low-overhead finite-state machine overlay for rapid fpga application development," in

International Workshop on Overlay Architectures for FPGAs (OLAF), co-located with FPGA 2017, 2017.

- [2] C. Pascoe, N. Kumar, H. Lam, and G. Stitt, "Fpga-pipelined discrete-event simulations for accelerated behavioral emulation of extreme-scale systems," in *Workshop on Modeling & Simulation of Systems & Applications (ModSim)*, 2016.
- [3] N. Kumar, C. Pascoe, C. Hajas, H. Lam, G. Stitt, and A. George, "Behavioral emulation for scalable design-space exploration of algorithms and architectures," in *International Conference on High Performance Computing*, pp. 5–17, 2016.
- [4] N. Kumar, A. George, H. Lam, G. Stitt, and S. Hammond, "Understanding performance and reliability trade-offs for extreme-scale systems using behavioral emulation," in *Workshop on Modeling & Simulation of Systems and Applications (ModSim)*, 2015.
- [5] A. Shastri, G. Stitt, and E. Riccio, "A scheduling and binding heuristic for high-level synthesis of fault-tolerant fpga applications," in *Application-specific Systems, Architectures and Processors (ASAP), 2015 IEEE 26th International Conference on*, pp. 202–209, July 2015.
- [6] D. Rudolph and G. Stitt, "An interpolation-based approach to multi-parameter performance modeling for heterogeneous systems," in *Application-specific Systems, Architectures and Processors (ASAP), 2015 IEEE 26th International Conference on*, pp. 174–180, July 2015.
- [7] J. Coole and G. Stitt, "Adjustable-cost overlays for runtime compilation," in *Field-Programmable Custom Computing Machines (FCCM), 2015 IEEE 23rd Annual International Symposium on*, pp. 21–24, May 2015.
- [8] A. Landy and G. Stitt, "Revisiting serial arithmetic: A performance and tradeoff analysis for parallel applications on modern fpgas," in *Field-Programmable Custom Computing Machines (FCCM), 2015 IEEE 23rd Annual International Symposium on*, pp. 9–16, May 2015.
- [9] J. Fowers, J. Liu, and G. Stitt, "A framework for dynamic parallelization of fpga-accelerated applications," in *Proceedings of the 17th International Workshop on Software and Compilers for Embedded Systems, SCOPES '14, (New York, NY, USA)*, pp. 1–10, ACM, 2014.
- [10] J. Fowers, K. Ovtcharov, K. Strauss, E. S. Chung, and G. Stitt, "A high memory bandwidth fpga accelerator for sparse matrix-vector multiplication," in *Proceedings of the 2014 IEEE 22nd International Symposium on Field-Programmable Custom Computing Machines, FCCM '14, (Washington, DC, USA)*, pp. 36–43, IEEE Computer Society, 2014.
- [11] J. Coole and G. Stitt, "Opencl high-level synthesis for mainstream fpga acceleration," in *Workshop on SoCs, Heterogeneous Architectures and Workloads (SHAW)*, feb 2014.
- [12] P. Cooke, J. Fowers, G. Stitt, and L. Hunt, "A comparison of correntropy-based feature tracking on fpgas and gpus," in *Application-Specific Systems, Architectures and Processors (ASAP), 2013 IEEE 24th International Conference on*, pp. 237–240, June 2013.
- [13] A. Landy and G. Stitt, "Pseudo-constant logic optimization," in *Application-Specific Systems, Architectures and Processors (ASAP), 2013 IEEE 24th International Conference on*, pp. 99–102, June 2013.
- [14] L. Hao and G. Stitt, "Virtual finite-state-machine architectures for fast compilation and portability," in *Application-Specific Systems, Architectures and Processors (ASAP), 2013 IEEE 24th International Conference on*, pp. 91–94, June 2013.
- [15] J. Fowers and G. Stitt, "Dynafuse: dynamic dependence analysis for FPGA pipeline fusion and locality optimizations," in *Proceedings of the ACM/SIGDA international symposium on Field programmable gate arrays, FPGA '13, (New York, NY, USA)*, pp. 201–210, ACM, February 2013.
- [16] A. Landy and G. Stitt, "A low-overhead interconnect architecture for virtual reconfigurable fabrics," in *CASES '12: Proceedings of the 2012 international conference on Compilers, architectures and synthesis for embedded systems, CASES '12, (New York, NY, USA)*, pp. 111–120, ACM, October 2012.
- [17] J. R. Wernsing, G. Stitt, and J. Fowers, "The racecar heuristic for automatic function specialization on multi-core heterogeneous systems," in *CASES '12: Proceedings of the 2012 international conference on Compilers, architectures and synthesis for embedded systems, CASES '12, (New York, NY, USA)*, pp. 81–90, ACM, October 2012.
- [18] J. Coole and G. Stitt, "BPR: fast FPGA placement and routing using macroblocks," in *CODES+ISSS '12: Proceedings of the eighth IEEE/ACM/IFIP international conference on Hardware/software codesign and system synthesis, CODES+ISSS '12, (New York, NY, USA)*, pp. 275–284, ACM, October 2012.
- [19] R. Kirchgessner, G. Stitt, A. George, and H. Lam, "VirtualRC: a virtual FPGA platform for applications and tools portability," in *FPGA '12: Proceedings of the ACM/SIGDA international symposium on Field Programmable Gate Arrays, FPGA '12, (New York, NY, USA)*, pp. 205–208, ACM, February 2012.
- [20] J. R. Wernsing and G. Stitt, "Racecar: a heuristic for automatic function specialization on multi-core heterogeneous systems," in *PPoPP '12: Proceedings of the 17th ACM SIGPLAN symposium on Principles and Practice of Parallel Programming, PPoPP '12, (New York, NY, USA)*, pp. 321–322, ACM, February 2012.
- [21] J. Fowers, G. Brown, P. Cooke, and G. Stitt, "A performance and energy comparison of FPGAs, GPUs, and multicores for sliding-window applications," in *FPGA '12: Proceedings of the ACM/SIGDA international symposium on Field Programmable Gate Arrays, FPGA '12, (New York, NY, USA)*, pp. 47–56, ACM, February 2012.
- [22] J. Curreri, G. Stitt, and A. George, "Communication visualization for bottleneck detection of high-level synthesis applications," in *FPGA '12: Proceedings of the ACM/SIGDA international symposium on Field Programmable Gate Arrays, FPGA '12, (New York, NY, USA)*, pp. 33–36, ACM, February 2012.
- [23] J. Wernsing and G. Stitt, "A scalable performance prediction heuristic for implementation planning on heterogeneous systems," in *ESTIMedia '10: 8th IEEE Workshop on Embedded Systems for Real-Time Multimedia*, pp. 71–80, October 2010.
- [24] J. Coole and G. Stitt, "Intermediate fabrics: Virtual architectures for circuit portability and fast placement and routing," in *CODES/ISSS '10: Proceedings of the IEEE/ACM/IFIP international conference on Hardware/Software codesign and system synthesis*, pp. 13–22, October 2010.

- [25] V. Aggarwal, C. Yoon, A. George, H. Lam, and G. Stitt, "Performance modeling for multilevel communication in shmem+," in *PGAS'10: Proceedings of the Conference on Partitioned Global Address Space Programming Model*, p. 10, October 2010.
- [26] C. Reardon, A. George, G. Stitt, and H. Lam, "An automated scheduling and partitioning algorithm for scalable rc systems," in *ERSA'10: Proceedings of the International Conference on Engineering of Reconfigurable Systems and Algorithms*, July 2010.
- [27] A. George, H. Lam, C. Pascoe, A. Lawande, and G. Stitt, "Novo-g: A view at the hpc crossroads for scientific computing," in *ERSA'10: Proceedings of the International Conference on Engineering of Reconfigurable Systems and Algorithms*, July 2010.
- [28] J. Wernsing and G. Stitt, "Elastic computing: A framework for transparent, portable, and adaptive multi-core heterogeneous computing," in *LCTES '10: Proceedings of the 2010 ACM SIGPLAN/SIGBED conference on Languages, compilers, and tools for embedded systems*, pp. 115–124, ACM, April 2010.
- [29] J. Curreri, G. Stitt, and A. George, "High-level synthesis techniques for in-circuit assertion-based verification," in *RAW '10: Proceedings of the 17th Reconfigurable Architectures Workshop*, April 2010.
- [30] J. Coole, J. Wernsing, and G. Stitt, "A traversal cache framework for fpga acceleration of pointer data structures: A case study on barnes-hut n-body simulation," in *Reconfigurable Computing and FPGAs, 2009. ReConFig '09. International Conference on*, pp. 143–148, Dec. 2009.
- [31] V. Aggarwal, R. Garcia, G. Stitt, A. George, and H. Lam, "Scf: a device- and language-independent task coordination framework for reconfigurable, heterogeneous systems," in *HPRCTA '09: Proceedings of the Third International Workshop on High-Performance Reconfigurable Computing Technology and Applications*, (New York, NY, USA), pp. 19–28, ACM, November 2009.
- [32] V. Aggarwal, A. George, K. Yalamanchili, C. Yoon, H. Lam, and G. Stitt, "Bridging parallel and reconfigurable computing with multilevel pgas and shmem+," in *HPRCTA '09: Proceedings of the Third International Workshop on High-Performance Reconfigurable Computing Technology and Applications*, (New York, NY, USA), pp. 47–54, ACM, November 2009.
- [33] G. Wang, G. Stitt, H. Lam, and A. D. George, "A framework for core-level modeling and design of reconfigurable computing algorithms," in *HPRCTA '09: Proceedings of the Third International Workshop on High-Performance Reconfigurable Computing Technology and Applications*, (New York, NY, USA), pp. 29–38, ACM, November 2009.
- [34] G. Stitt, G. Chaudhari, and J. Coole, "Traversal caches: a first step towards FPGA acceleration of pointer-based data structures," in *CODES/ISSS '08: Proceedings of the 6th IEEE/ACM/IFIP international conference on Hardware/Software codesign and system synthesis*, (New York, NY, USA), pp. 61–66, ACM, October 2008.
- [35] S. Merchant, B. Holland, C. Reardon, A. George, H. Lam, G. Stitt, M. Smith, N. Alam, I. Gonzalez, E. El-Araby, P. Saha, T. El-Ghazawi, and H. Simmler, "Strategic challenges for application development productivity in reconfigurable computing," in *IEEE National Aerospace and Electronics Conference (NAECON)*, July 2008.
- [36] I. Gonzalez, E. El-Araby, P. Saha, T. El-Ghazawi, H. Simmler, S. Merchant, B. Holland, C. Reardon, A. George, H. Lam, G. Stitt, N. Alam, and M. Smith, "Classification of application development for FPGA-based systems," in *IEEE National Aerospace and Electronics Conference (NAECON)*, July 2008.
- [37] G. Stitt and J. Villarreal, "Recursion flattening," in *GLSVLSI '08: Proceedings of the 18th ACM Great Lakes symposium on VLSI*, (New York, NY, USA), pp. 131–134, ACM, May 2008.
- [38] G. Stitt, "Hardware/software partitioning with multi-version implementation exploration," in *GLSVLSI '08: Proceedings of the 18th ACM Great Lakes symposium on VLSI*, (New York, NY, USA), pp. 143–146, ACM, May 2008.
- [39] S. Sirowy, G. Stitt, and F. Vahid, "C is for circuits: capturing FPGA circuits as sequential code for portability," in *FPGA '08: Proceedings of the 16th international ACM/SIGDA symposium on Field programmable gate arrays*, (New York, NY, USA), pp. 117–126, ACM, February 2008.
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- [41] G. Stitt, F. Vahid, and W. Najjar, "A code refinement methodology for performance-improved synthesis from C," in *ICCAD '06: Proceedings of the 2006 IEEE/ACM international conference on Computer-aided design*, (New York, NY, USA), pp. 716–723, ACM, November 2006.
- [42] G. Stitt and F. Vahid, "New decompilation techniques for binary-level co-processor generation," in *ICCAD '05: Proceedings of the 2005 IEEE/ACM International conference on Computer-aided design*, (Washington, DC, USA), pp. 547–554, IEEE Computer Society, November 2005.
- [43] G. Stitt, F. Vahid, G. McGregor, and B. Einloth, "Hardware/software partitioning of software binaries: a case study of h.264 decode," in *CODES+ISSS '05: Proceedings of the 3rd IEEE/ACM/IFIP international conference on Hardware/software codesign and system synthesis*, (New York, NY, USA), pp. 285–290, ACM, September 2005.
- [44] G. Stitt and F. Vahid, "A decompilation approach to partitioning software for microprocessor/FPGA platforms," in *DATE '05: Proceedings of the conference on Design, Automation and Test in Europe*, (Washington, DC, USA), pp. 396–397, IEEE Computer Society, March 2005.
- [45] G. Stitt, Z. Guo, W. Najjar, and F. Vahid, "Techniques for synthesizing binaries to an advanced register/memory structure," in *FPGA '05: Proceedings of the 2005 ACM/SIGDA 13th international symposium on Field-programmable gate arrays*, (New York, NY, USA), pp. 118–124, ACM, February 2005.
- [46] G. Stitt, R. Lysecky, and F. Vahid, "Dynamic hardware/software partitioning: a first approach," in *DAC '03: Proceedings of the 40th conference on Design automation*, (New York, NY, USA), pp. 250–255, ACM, June 2003.
- [47] D. C. Suresh, W. A. Najjar, F. Vahid, J. R. Villarreal, and G. Stitt, "Profiling tools for hardware/software partitioning of embedded applications," in *LCTES '03: Proceedings of the 2003 ACM SIGPLAN conference on Languages, compilers, and tools for embedded systems*, (New York, NY, USA), pp. 189–198, ACM, June 2003.

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- [50] G. Stitt, B. Grattan, J. Villarreal, and F. Vahid, "Using on-chip configurable logic to reduce embedded system software energy," in *FCCM '02: Proceedings of the 10th Annual IEEE Symposium on Field-Programmable Custom Computing Machines*, (Washington, DC, USA), pp. 143–151, IEEE Computer Society, April 2002.
- [51] G. Stitt, F. Vahid, T. Givargis, and R. Lysecky, "A first-step towards an architecture tuning methodology for low power," in *CASES '00: Proceedings of the 2000 international conference on Compilers, architecture, and synthesis for embedded systems*, (New York, NY, USA), pp. 187–192, ACM, November 2000.

Technical Reports

- [1] G. Stitt and F. Vahid. Binary-level hardware/software partitioning of MediaBench, NetBench, and EEMBC benchmarks. Tech. Rep. UCR-CSE-03-01, University of California, Riverside, January 2003.

Funding

- ❖ NSF Center for High-Performance Reconfigurable Computing (CHREC) *FPGA Virtualization & Application Case Studies*, \$120,000, January 2017-December 2017, PI: **G. Stitt**, Co-PI: A. Gordon-Ross
- ❖ Harris Endowed Seed Fund. *Thermal Aware Computing: Hardware Monitoring and Software Controls*, \$40,000, January 2016-December 2018, PI: **G. Stitt**, Co-PI: S. Ranka
- ❖ NSF Center for High-Performance Reconfigurable Computing (CHREC), *Virtualization-Enabled FPGA Optimizations*, \$152,000, January 2016-December 2016, PI: **G. Stitt**, Co-PI: A. Gordon-Ross
- ❖ NSF Center for High-Performance Reconfigurable Computing (CHREC), *VAPoR – Virtualization for Adaptivity, Productivity, Portability, and Redundancy*, \$120,000, January 2015-December 2015, PI: **G. Stitt**, Co-PI: A. Gordon-Ross
- ❖ NSF Center for High-Performance Reconfigurable Computing (CHREC), *FPGA and Many-Core Computing for Aerospace and Defense*, \$172,000, January 2015-December 2015, PI: A. George, Co-PI: H. Lam, **G. Stitt**
- ❖ DOE/NNSA, *Novo-G Exascale Emulation (NGEE) program, PSAAP-II Center for Compressible Multiphase Turbulence*, \$10M (total), \$2.214M (NGEE portion), December 2013-January 2019, PI: A. George, Co-PI: H. Lam and **G. Stitt**
- ❖ NSF Center for High-Performance Reconfigurable Computing (CHREC), *High-Productivity Design Automation for FPGA Applications*, \$80,000, January 2014-December 2014, PI: **G. Stitt**
- ❖ NSF Center for High-Performance Reconfigurable Computing (CHREC), *Advanced Computing for Aerospace and Defense*, \$158,000, January 2014-December 2014, PI: A. George, Co-PI: H. Lam, **G. Stitt**
- ❖ NSF Center for High-Performance Reconfigurable Computing (CHREC), *Virtualization Strategies for Fast FPGA Compilation*, \$76,000, January 2013-December 2013, PI: **G. Stitt**
- ❖ NSF Center for High-Performance Reconfigurable Computing (CHREC), *Reconfigurable & Many-core Computing for Aerospace & Defense*, \$208,000, January 2013-December 2013, PI: A. George, Co-PI: H. Lam, **G. Stitt**
- ❖ **National Science Foundation CAREER Award**, CNS-1149285, *Design Virtualization for Mainstream Programming of Reconfigurable Computers*, \$450,000, February 2012-January 2017, PI: **G. Stitt**
- ❖ NSF Center for High-Performance Reconfigurable Computing (CHREC), *A Unified Design Stack for Productivity - from Modeling to Middleware*, \$161,000, January 2012-December 2012, PI: A. George, Co-PI: H. Lam, **G. Stitt**
- ❖ NSF Center for High-Performance Reconfigurable Computing (CHREC), *Rapid Application Design and Compilation for FPGAs*, \$66,500, January 2012-December 2012, PI: **G. Stitt**
- ❖ NSF Center for High-Performance Reconfigurable Computing (CHREC), *Tools Research for Application Design Productivity*, \$173,000, January 2011-December 2011, PI: **G. Stitt**, Co-PI: A. George, H. Lam
- ❖ NSF Center for High-Performance Reconfigurable Computing (CHREC), *Applications Research for RC Systems*, \$183,000, January 2011-December 2011, PI: H. Lam, Co-PI: A. George, **G. Stitt**
- ❖ NSF Center for High-Performance Reconfigurable Computing (CHREC), *Hardware Virtualization Layer for Ubiquitous RC*, \$84,000, January 2010-December 2010, PI: **G. Stitt**, Co-PI: A. George
- ❖ NSF Center for High-Performance Reconfigurable Computing (CHREC), *Comprehensive Framework for Application Development Productivity*, \$118,000, January 2010-December 2010, PI: A. George, Co-PIs: H. Lam and **G. Stitt**
- ❖ National Science Foundation, CNS-0914474, *CSR: Small: Elastic Computing - An Enabling Technology for Transparent, Portable, and Adaptive Multi-Core Heterogeneous Computing*, \$405,362, August 2009-July 2012, PI: **G. Stitt**
- ❖ NSF Center for High-Performance Reconfigurable Computing (CHREC), *Translation and Execution Productivity*, \$52,000, January

2009-December 2009, PI: **G. Stitt**, Co-PI: A. George

- ❖ NSF Center for High-Performance Reconfigurable Computing (CHREC), *System-Level Formulation and Design*, \$140,000, January 2009-December 2009, PI: A. George, Co-PIs: H. Lam and **G. Stitt**

Awards

- ❖ University of Florida College of Engineering *Undergraduate Teacher of the Year* (2014-2015 Academic Year)
- ❖ **National Science Foundation CAREER Award**, CNS-1149285, *Design Virtualization for Mainstream Programming of Reconfigurable Computers*, \$450,000, February 2012-January 2017, PI: **G. Stitt**

Donations

- ❖ Altera Corporation, Terasic DE2-70 FPGA Development Board, February 2009, Commercial Value: \$599