

# Greg Stitt

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Research Interests Reconfigurable computing: emphasis in synthesis, compilers, embedded systems, hardware/software co-design, low power-design, system-on-a-chip multi-core architectures, real-time systems, and run-time optimizations.

Education 2000-2007 University of California, Riverside  
Ph.D. Computer Science

- Advisor: Dr. Frank Vahid

1996-2000 University of California, Riverside  
B.S. Computer Science

- GPA: 3.953, Graduated Summa Cum Laude

Employment Assistant Professor  
University of Florida, Dept. of Electrical and Computer Engineering  
August 2007 to current

Teaching experience

- EEL4930/EEL5934 (Reconfigurable Computing) – Assistant Professor, UF (Fall 2007)
- CS 161L (Computer Architecture) – Lecturer, UCR (Spring 2005)
- CS 161 (Computer Architecture) - Teaching assistant, UCR (Fall 2001)
- CS 122A (Embedded Systems) - Teaching assistant, UCR (Fall 2000, 2003)
- CS 122B (Adv. Embedded Systems) - Teaching assistant, UCR (Winter 2003, 2004)
- Computer science tutor, UCR (1999)

Patents

1. **Warp Processor for Dynamic Hardware/Software Partitioning**  
F. Vahid, R. Lysecky, G. Stitt. Patent Pending, 2004.

Publications *Journal Publications*

1. **Propagating Constants Past Software to Hardware Peripherals in Fixed-Application Embedded Systems**  
F. Vahid, R. Patel and G. Stitt  
Special Issue of ACM SIGARCH Newsletter, Dec. 2001. Selected for special issue from earlier version of paper in Compilers and Operating Systems for Low Power (COLP'01).
2. **The Energy Advantages of Microprocessor Platforms with On-Chip Configurable Logic**  
G. Stitt and F. Vahid  
IEEE Design and Test of Computers, November 2002, Volume 19, Issue 6, pp. 36-43.
3. **Improving Software Performance with Configurable Logic**  
J. Villarreal, D. Suresh, G. Stitt, F. Vahid and W. Najjar  
Kluwer Journal on Design Automation of Embedded Systems, November 2002, Volume 7, Issue 4, pp. 325-339.
4. **Energy Savings and Speedups From Partitioning Critical Software Loops to Hardware in Embedded Systems.**  
G. Stitt, F. Vahid, S. Nematbakhsh  
Transactions on Embedded Computing Systems (TECS), February 2004, Volume 3, Issue 1, pp. 218-232.
5. **Highly Configurable Platforms for Embedded Computing Systems**  
F. Vahid, R. Lysecky, C. Zhang and G. Stitt  
Microelectronics Journal, November 2003, Volume 34, Issue 11, pp. 1025-1029.

6. **Warp Processors**  
R. Lysecky, G. Stitt, F. Vahid.  
ACM Transactions on Design Automation of Electronic Systems (TODAES), 2006,  
Volume 11, Number 3, pp. 659 - 681.
7. **Binary Synthesis**  
G. Stitt, F. Vahid  
ACM Transactions on Design Automation of Electronic Systems (TODAES), August 2007,  
Volume 12, Number 3
8. **Warp Processing: Dynamic Translation of Binaries to FPGA Circuits**  
F. Vahid, G. Stitt, R. Lysecky  
Submitted to IEEE Computer

### *Book Chapters*

1. **Propagating Constants Past Software to Hardware Peripherals in Fixed-Application Embedded Systems**  
G. Stitt and F. Vahid  
Compilers and Operating Systems for Low Power. Kluwer Academic Publishers, 2002.
2. **Hardware/Software Partitioning**  
F. Vahid, G. Stitt  
To be published in Reconfigurable Computing: The Theory and Practice of FPGA-Based Computation

### *Conference Publications*

1. **A First-step Towards an Architecture Tuning Methodology for Low Power**  
G. Stitt, F. Vahid, T. Givargis, R. Lysecky  
IEEE/ACM Conference on Compilers, Architectures, and Synthesis for Embedded Systems (CASES), 2000, pp.187-192.
2. **Using On-Chip Configurable Logic to Reduce Embedded System Software Energy**  
G. Stitt, B. Grattan, J. Villarreal and F. Vahid  
IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM), 2002, pp. 143-151.
3. **Codesign-Extended Applications**  
B. Grattan, G. Stitt and F. Vahid  
IEEE/ACM International Symposium on Hardware/Software Codesign (CODES), 2002, pp. 1-6.
4. **Hardware/Software Partitioning of Software Binaries**  
G. Stitt and F. Vahid  
IEEE/ACM International Conference on Computer Aided Design (ICCAD), 2002, pp. 164-170.
5. **Profiling Tools for Hardware/Software Partitioning of Embedded Applications**  
D. Suresh, W. Najjar, F. Vahid, J. Villarreal, G. Stitt  
ACM Conference on Languages, Compilers and Tools for Embedded Systems (LCTES), 2003, pp. 189-198.
6. **Dynamic Hardware/Software Partitioning: A First Approach**  
G. Stitt, R. Lysecky and F. Vahid  
IEEE/ACM Conference on Design Automation (DAC), 2003, pp. 250-255.
7. **Techniques for Synthesizing Binaries to an Advanced Register/Memory Structure**  
G. Stitt, Z. Guo, F. Vahid, W. Najjar  
ACM/SIGDA International Symposium on Field Programmable Gate Arrays (FPGA), 2005, pp. 118-124.
8. **A Decompile Approach to Partitioning Software for Microprocessor/FPGA Platforms**  
G. Stitt and F. Vahid  
IEEE/ACM Design Automation and Test in Europe (DATE), 2005, pp. 396-397.
9. **Hardware/Software Partitioning of Software Binaries: A Case Study of H.264 Decode**  
G. Stitt, F. Vahid, G. McGregor, B. Einloth  
IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES/ISSS), 2005, pp. 285-290.
10. **New Decompile Techniques for Binary-level Co-processor Generation**  
G. Stitt, F. Vahid  
IEEE/ACM International Conference on Computer Aided Design (ICCAD), 2005, pp. 547-554.
11. **A Code Refinement Methodology for Performance-Improved Synthesis from C**  
G. Stitt, F. Vahid, W. Najjar  
IEEE/ACM International Conference on Computer Aided Design (ICCAD), 2006.
12. **Thread Warping: A Framework for Dynamic Synthesis of Thread Accelerators**  
G. Stitt, F. Vahid

- IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES/ISSS), 2007.
13. **Hardware Software Partitioning with Multi-Version Implementation Exploration**  
G. Stitt, F. Vahid  
To be submitted to IEEE/ACM Conference on Design Automation (DAC), 2008.
  14. **Recursion Flattening for Improved High-Level Synthesis**  
G. Stitt, J. Villarreal, D. Sheldon, F. Vahid  
To be submitted to IEEE/ACM Conference on Design Automation (DAC), 2008.
  15. **Expandable Logic**  
G. Stitt, F. Vahid  
Submitted to ACM/SIGDA International Symposium on Field Programmable Gate Arrays (FPGA), 2008.

### Technical Reports

1. **Binary-Level Hardware/Software Partitioning of MediaBench, NetBench, and EEMBC Benchmarks**  
G. Stitt and F. Vahid  
Technical Report UCR-CSE-03-01. January 2003.

### Professional activities

- **Presentation at UC Berkeley ESD Seminar.** Warp processors. March 2004.
- **Presentation at NEC.** Hardware/software partitioning of software binaries. July 2001.
- Presented papers at ICCAD 2002, DAC 2003, FCCM 2002, FPGA 2005, CODES/ISSS 2005, ICCAD 2005, ICCAD 2006.
- Reviewer, IEEE/ACM International Conference on Computer Aided Design (ICCAD), 2006.
- Reviewer, IEEE/ACM International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES), 2003, 2005.
- Reviewer, IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), 2003, 2005.
- Reviewer, ACM Conference on Languages, Compilers, and Tools for Embedded Systems (LCTES), 2003.
- Reviewer, International Symposium on High-Performance Computer Architecture (HPCA), 2007.
- Reviewer, IEEE Transactions on Parallel and Distributed Systems Manuscript (TPDS), 2006.
- Member of IEEE

### Computer skills

- Languages: C/C++, Java, Perl, VHDL, SystemC, Visual Basic
- Operating Systems: Windows, Linux, Unix, VxWorks
- Tools: Synopsis Design Compiler, Synopsis Behavioral Compiler, Keil, Xilinx ISE, Xilinx Platform Studio, Xilinx Xpower, Tornado, Triscend E5/A7 Fast Chip, Synplicity Synplify, SimpleScalar, Wattach
- Platforms: Xilinx Virtex II Pro, Triscend E7/A7

### Awards received

- GAANN Fellowship
- UCR Chancellor's Fellowship
- Summa Cum Laude
- Travel Grant (CASES 2003)
- Dean's List
- Golden Key National Honor Society
- Scholastic Achievement Award for GPA over 3.9

### Projects

#### Synthesis/Partitioning Tool for Software Binaries

June 2002 to current

University of California, Riverside

Designed a synthesis tool that creates register-transfer level hardware based on a software binary. The tool first decompiles the software binary to recover high-level information suitable for synthesis. The tool then performs behavioral synthesis on the decompiled representation, creating a register-transfer representation in VHDL.

#### Cycle-Accurate MIPS Microprocessor Simulator

Fall 2001

University of California, Riverside

Created a cycle-accurate simulator for a pipelined processor. The processor's instruction set was similar to a MIPS. Simulator provided statistics such as CPI (cycles per instruction), cache

performance, and execution time.

### Optimizations for Intel 8051 VHDL Soft Core

June 2000 to June 2001

University of California, Riverside

Performed architectural optimizations to Intel 8051 VHDL soft core to reduce power/energy consumption. Architectural modifications included controller partitioning, guarded evaluations, bus encoding, state encoding, and clock gating.

### E-book

January 1999 to March 1999

Dr. Frank Vahid

University of California, Riverside

Designed electronic book that allows text documents to be stored and read. Documents can be downloaded from any PC using the serial port. An LCD displayed the stored text. Designed to be cheap and to consume very little power. Involved embedded system design, 8051 microprocessor programming, VHDL programming, FPGA prototyping, and serial communication.

## Professional experience

### Graduate Student Researcher

June 2000 to June 2007

University of California, Riverside

Performed research in hardware/software partitioning and synthesis of software binaries. Researched architecture and on-chip tools for Warp processors, which are capable of dynamically optimizing software by performing hardware/software partitioning at run time.

### Teaching Assistant

Fall 2000 to current

University of California, Riverside

Instructed students during labs for classes dealing with computer architecture and embedded systems. Responsible for developing labs, grading assignments, and occasionally giving lectures.

### Software and Multimedia Designer

April 1998 to January 1999

Automated Pathology Systems

Grand Terrace, CA

Programmed medical software products. Provided quality assurance testing and customer technical support. Also, provided web site and multimedia design, including full CD demos of the company's products.

### Tutor

September 1998 to June 1999

University of California Riverside Learning Center

Responsible for tutoring college students in Physics, Math, and Computer Science. Provided services to computer science students with regard to basic programming fundamentals, data structures, algorithms, and digital design.

### Computer Science Grader

September 1999 to June 2000

University California at Riverside

Responsible for grading programming assignments, homework, and tests in undergraduate computer science classes.