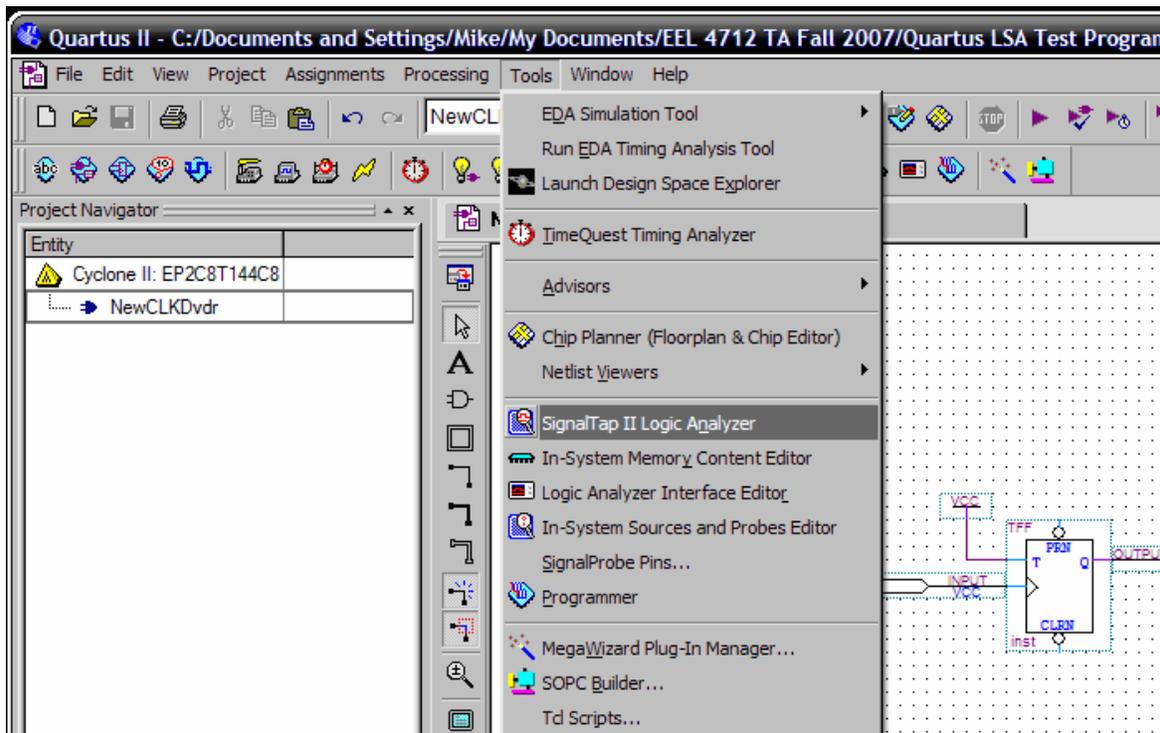


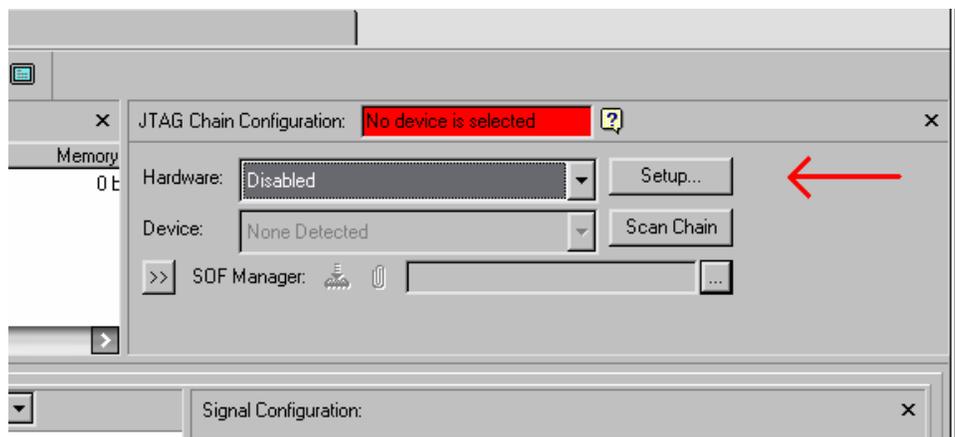
Tutorial for Quartus' SignalTap II Logic Analyzer

After successfully compiling a completed project and setting pin assignments, select SignalTap II Logic Analyzer from the tools dropdown menu (as shown below). Ensure the JTAG programmer (ByteBlaster) is connected between the board and the computer, and that the UF-4712 board has power. (You can also open the SignalTap II Logic Analyzer by selecting "File | New | Other Files | SignalTapII Logic Analyzer File".)



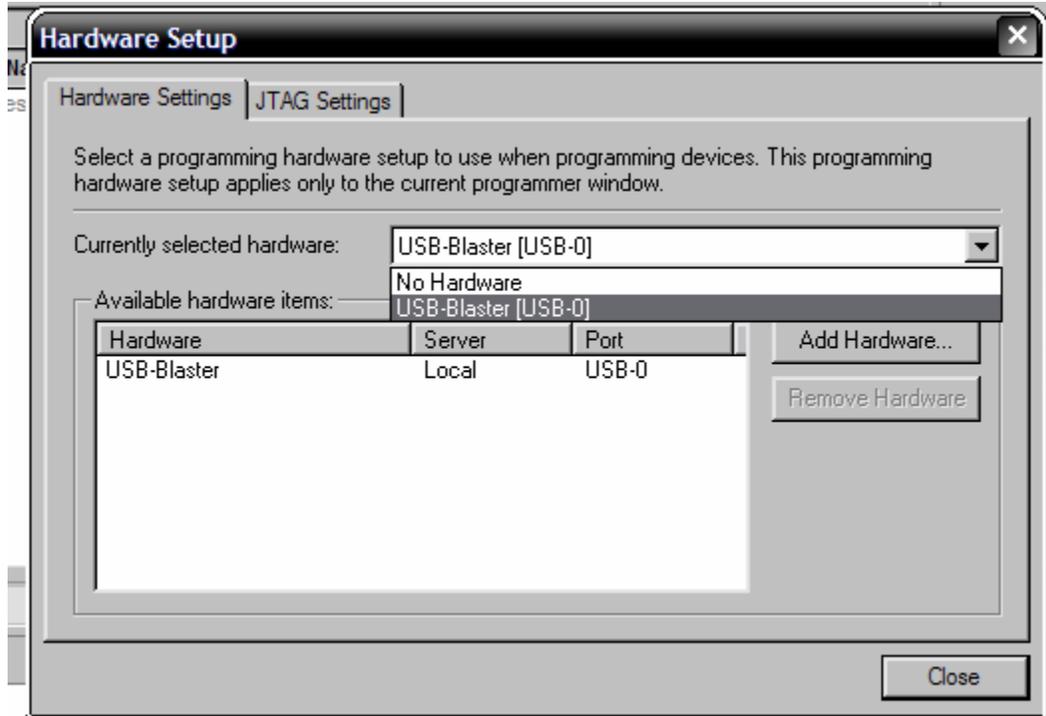
Note: If you receive an error saying "SignalTap not available under the current license," you need to enable "TalkBack." Go to Tools | Options. Find Internet Connectivity under the General heading. Click the button that says "TalkBack Options." Check the box for "Turn on TalkBack feature." Click OK to both dialog boxes and restart Quartus.

Once SignalTap has opened, look under the JTAG Chain Configuration, select Setup, as shown below.

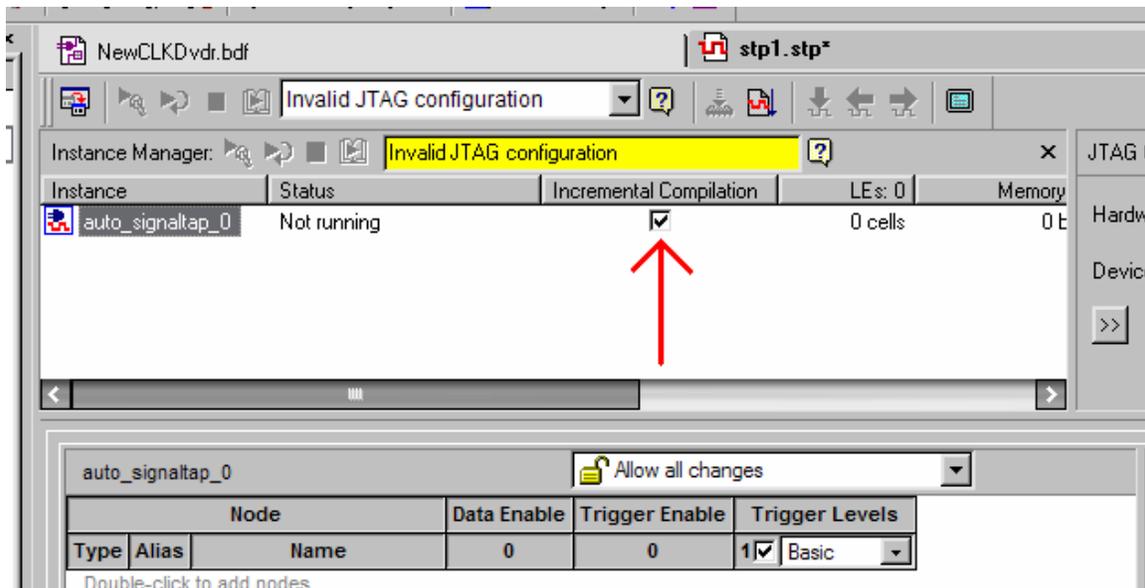


Tutorial for Quartus' SignalTap II Logic Analyzer

In Hardware Setup, select the programmer used to program the FPGA, just as when first connecting the programmer.

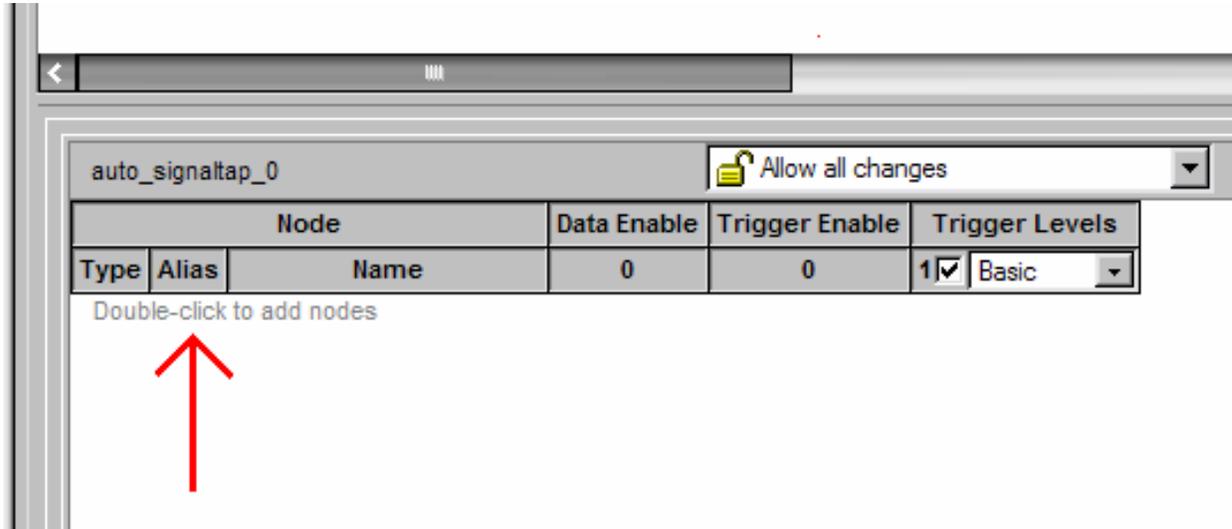


Under the Instance Manager, uncheck the Incremental Compilation. Click OK to the warning that pops up (about the clock and nodes being changed pre-synthesis).

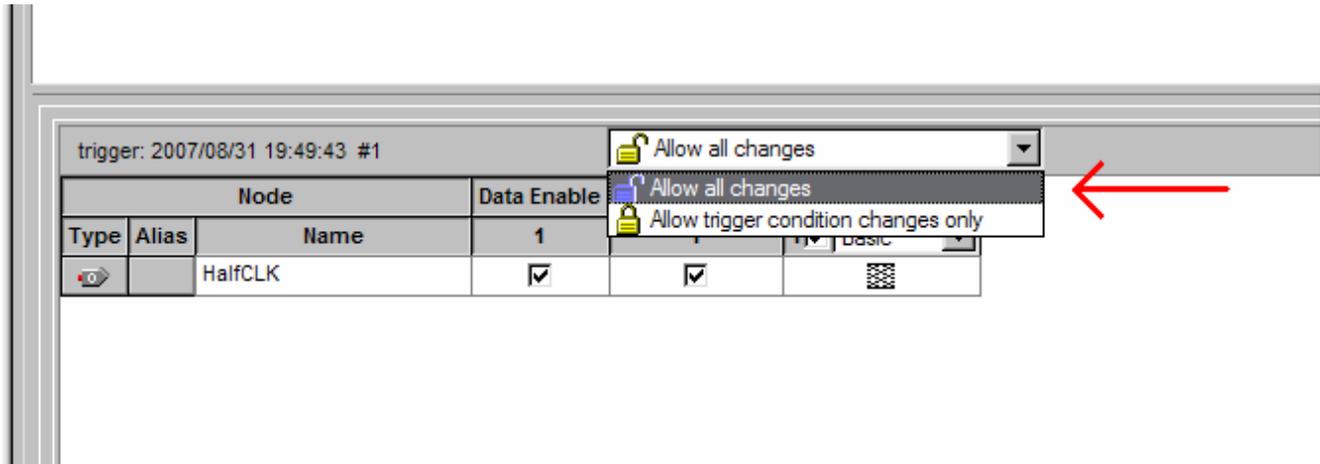


Tutorial for Quartus' SignalTap II Logic Analyzer

Under the instance, double click to add all the nodes to be analyzed.

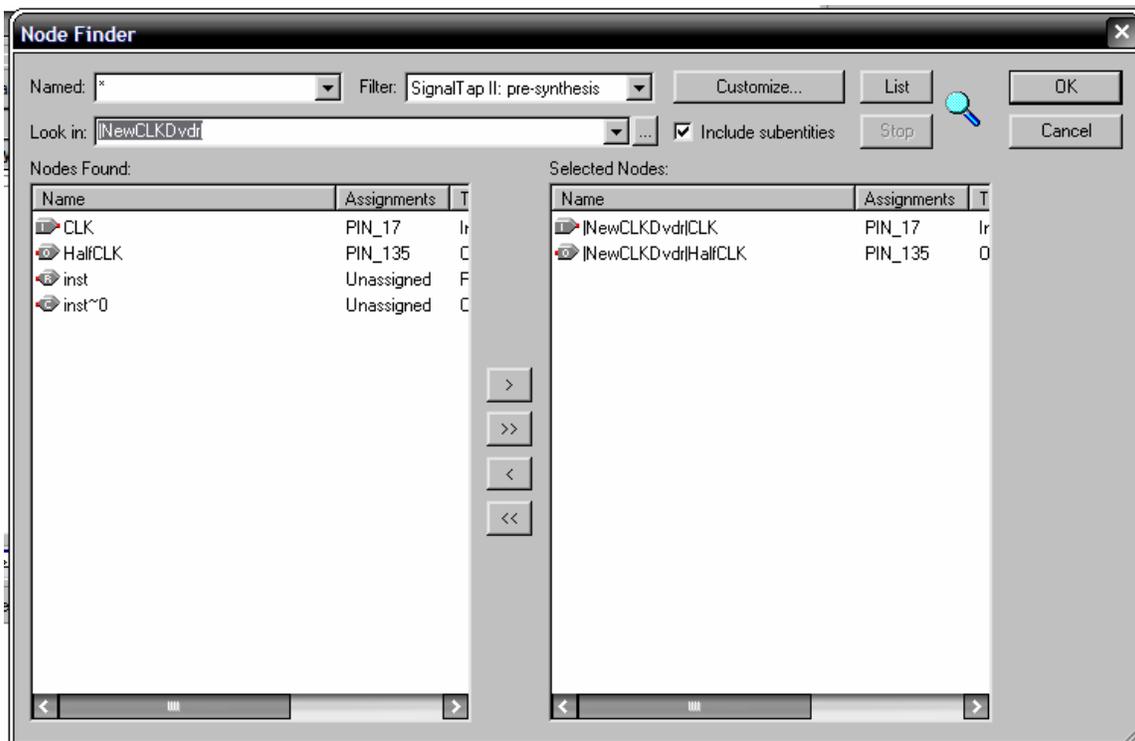


Set the trigger to allow all changes. This allows you to manually select the clock.



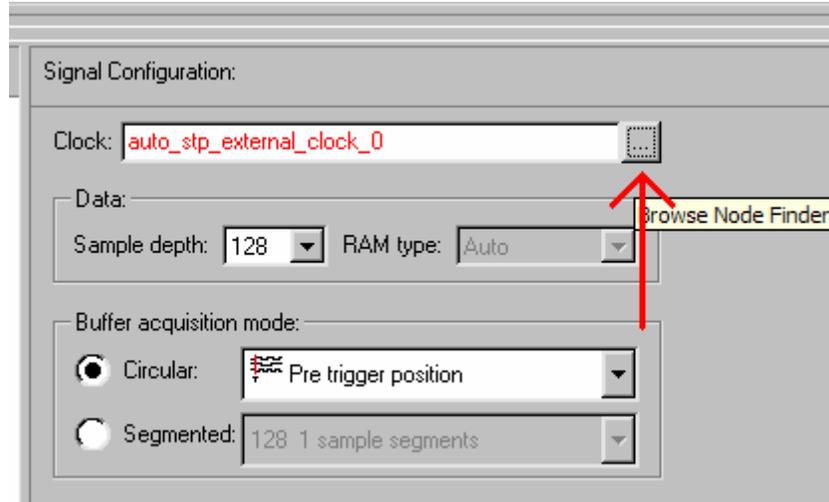
Tutorial for Quartus' SignalTap II Logic Analyzer

Add the signals to be analyzed exactly as in the simulation waveform. Click OK.

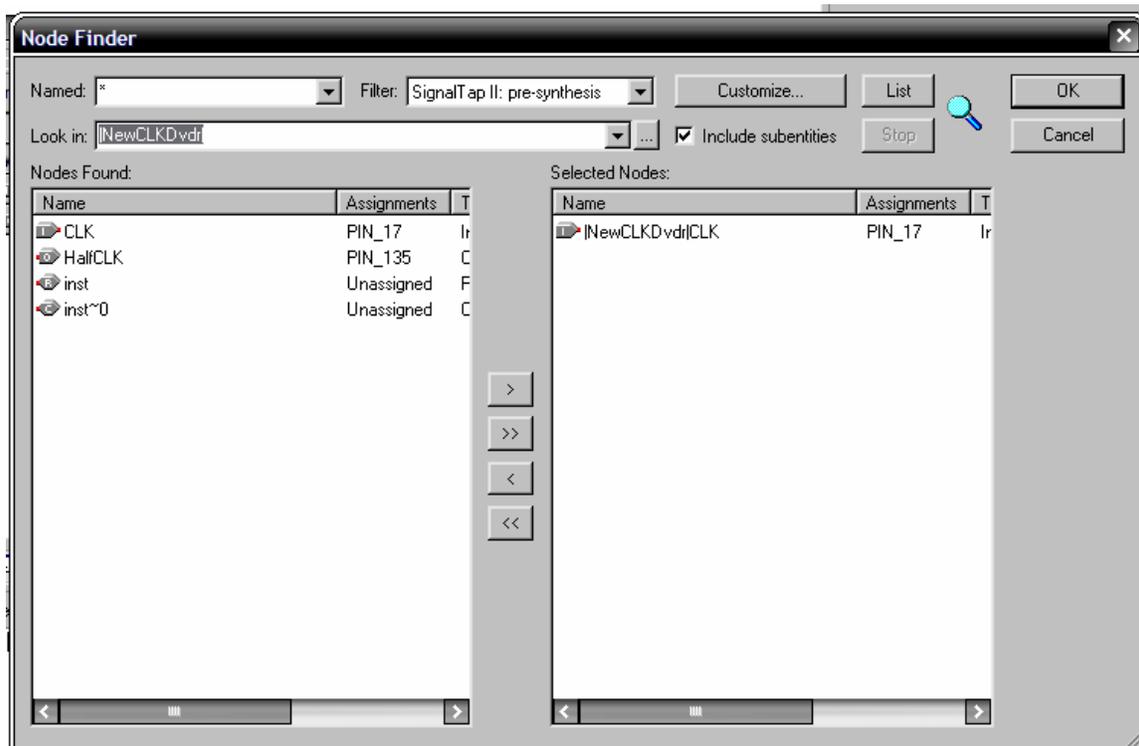


Tutorial for Quartus' SignalTap II Logic Analyzer

Under Signal Configuration, the clock must be set to the FPGA clock. Click the browse button next to the Clock.

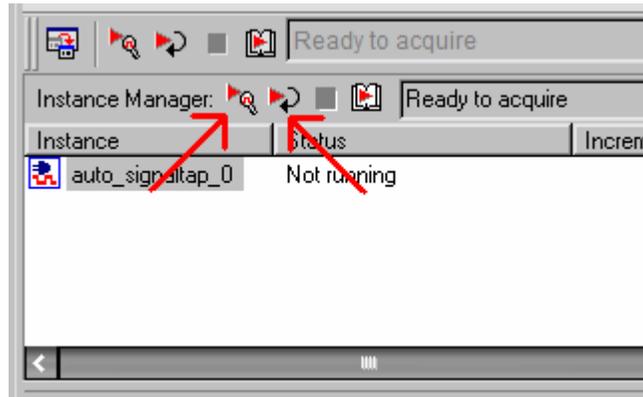


List all the pins then select the CLK input at Pin 17.

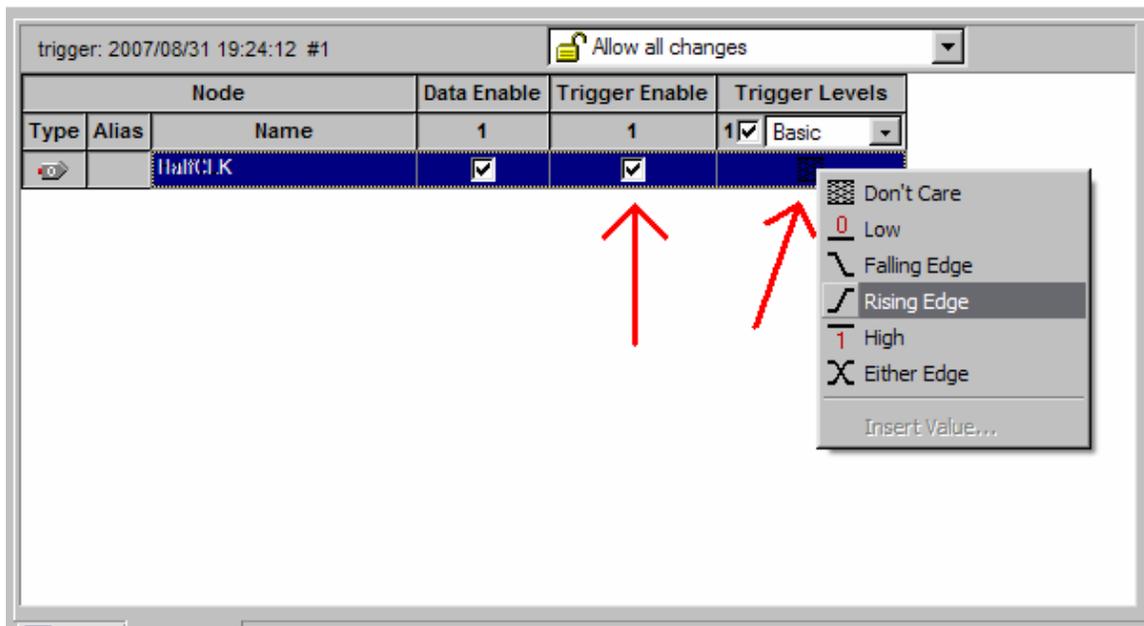


Tutorial for Quartus' SignalTap II Logic Analyzer

The signal used for the Clock cannot be analyzed, and is removed from the list if it was there. Recompile the project. Program the FPGA as usual. Go back to the SignalTap Analyzer. Click Autorun Analysis to continuously update the waveform or click Run Analysis to obtain a single waveform.



To set up a trigger, ensure the trigger enable is checked for the desired signal then right click on the trigger level then choose the desired trigger level.



Tutorial for Quartus' SignalTap II Logic Analyzer

To create a text file of the data, right click in the white space below the waveform and select Create SignalTap II List File.

