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Tutorial for	Ouartus' SignalTap II Log	zic Analyzer

After successfully compiling a completed project and setting pin assignments, select SignalTap II Logic Analyzer from the tools dropdown menu (as shown below). Ensure the JTAG programmer (ByteBlaster) is connected between the board and the computer, and that the UF-4712 board has power. (You can also open the SignalTap II Logic Anayzer by selecting "File | New | Other Files | SignalTapII Logic Anayzer File".)



Note: If you receive an error saying "SignalTap not available under the current license," you need to enable "TalkBack." Go to Tools | Options. Find Internet Connectivity under the General heading. Click the button that says "TalkBack Options." Check the box for "Turn on TalkBack feature." Click OK to both dialog boxes and restart Quartus.

Once SignalTap has opened, look under the JTAG Chain Configuration, select Setup, as shown below.

×	JTAG Chain Configuration: No device is selected	×
Memory 0 E	Hardware: Disabled Setup	
	Device: None Detected Scan Chain	
	>> SOF Manager: 📩 🕧 🛄	
>		
-	Signal Configuration:	×

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In Hardware Setup, select the programmer used to program the FPGA, just as when first connecting the programmer.

Se hai	lect a programming hardware rdware setup applies only to I	e setup to use whe the current progra	en programming dev mmer window.	ices. This programming
Cu	rrently selected hardware:	USB-Blaster [L	ISB-0]	-
	Available hardware items:	No Hardware USB-Blaster [U	ISB-0]	
	Hardware	Server	Port	Add Hardware
	USB-Blaster	Local	USB-0	Remove Hardware

Under the Instance Manager, uncheck the Incremental Compilation. Click OK to the warning that pops up (about the clock and nodes being changed pre-synthesis).

-	1 -	_		- 1 -	•			- I					
د 11	R	Nev	wCLKDiv	/dr.bdf) 1	n stp1	.stp*			
1]6	₽ ►	ą 🔊		Invalid JTA	G con	figuration	▼ 🤉 ,	÷. 🖸	1 🗄 🖶 🖈			
ł	Ins	tance	Manage	er: 🍡 I	> ∎ 🛙	Invalid.	JTAG config	uration		2		×	JTAG C
1	Ins	tance			Status		1	ncremental Compi	lation	LE s: 0	Me	emory	
1		auto_	signalta	р_0	Not running					0 cells		OE	Hardw
								$ \wedge$					Device
													>> 9
1								- I.					
1	<	_			uu							\geq	
1													
1		auto_	signalta	ip_0				Allow all ch	anges		•		
	Γ			Nod	le		Data Enable	Trigger Enabl	e Trig	gger Levels			
	- F	Гуре	Alias		Name		0	0	1	Basic 💽			
1		Doub	le click	to add n	odes								

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Under the instance, double click to add all the nodes to be analyzed.

<		_	WA	_			
	auto_	signalta	ap_0		Allow all chan	ges	•
			Node	Data Enable	Trigger Enable	Trigger Levels	
	Туре	Alias	Name	0	0	1 Basic -	
	Doub		to add nodes				

Set the trigger to allow all changes. This allows you to manually select the clock.

trigge	er: 2007	7/08/31 19:49:43 #1		🔒 Allow all chan	ges	· ,
		Node	Data Enable	Allow all chang	ges	\rightarrow
Туре	Alias	Name	1	Allow trigger c	ondition changes only	
•		HalfCLK	N	N		

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Add the signals to be analyzed exactly as in the simulation waveform. Click OK.

Į	Node Finder			×
3	Named: ×	Filter: SignalTap II: pre-	ynthesis 💌 Customize	List OK
	Look in: NewCLKDvdr		✓ ✓ Include subentities	Stop Cancel
4	Nodes Found:		Selected Nodes:	
1	Name	Assignments T	Name	Assignments T
	CLK CLK	PIN_17 Ir	INewCLKD vdr/CLK	PIN_17 Ir
	💿 HalfCLK	PIN_135 C	🐵 NewCLKDvdr/HalfCLK	PIN_135 0
	🔹 🐨 inst	Unassigned F		
	💿 inst~0	Unassigned C		
		>>		
		<		
J.				
1				
1				
	<	>	<	>

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Under Signal Configuration, the clock must be set to the FPGA clock. Click the browse button next to the Clock.

Signal Configuration:	
Clock: auto_stp_external_clock_0	
Data: Sample depth: 128 v RAM type: Auto	Browse Node Finder
Buffer acquisition mode:	
Circular: Fre trigger position	-
Segmented: 128 1 sample segments	T

List all the pins then select the CLK input at Pin 17.

Node Finder							
	Named: 🛛	Filter: Signal	Fap II: pre-sy	nthesis 💌 Customize	List 🔾	ОК	
	Look in: NewCLKDvdr			💽 🔽 Include subentities	Stop	Cancel	
	Nodes Found:			Selected Nodes:			
	Name	Assignments	Ī	Name	Assignments T		
	CLK	PIN_17	lr 🛛		PIN_17 Ir		
	HalfCLK	PIN_135	C I				
	I mst	Unassigned	F				
		Unassigned	L .				
			\rightarrow				
	<	>		<	>		

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The signal used for the Clock cannot be analyzed, and is removed from the list if it was there. Recompile the project. Program the FPGA as usual. Go back to the SignalTap Analyzer. Click Autorun Analysis to continuously update the waveform or click Run Analysis to obtain a single waveform.

🛛 🗃 🍬 ⊳ 🔳 😭 Ready to acquire	
Instance Manager: 🍬 📭 🔛 Ready to acquire	
Instance Islatus	Increme
auto_signattap_0 Not ruening	
K	

To set up a trigger, ensure the trigger enable is checked for the desired signal then right click on the trigger level then choose the desired trigger level.

-

trigger: 2007/08/31 19:24:12 #1				Allow all changes			
Node		Data Enable	Trigger Enable	Trigger Levels			
Туре	Alias	Name	1	1	1 Basic -		
		HalfCLK			St Don't Care		
				\uparrow	Image: Source date Image: Define edge Image: Define edge		

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To create a text file of the data, right click in the white space below the waveform and select Create SignalTap II List File.

log: 2007/08	3/31 19:49:43 #2					click to inser
Type Alias	Name HalfCLK	-16 -8 [/////////		8, 16		32
		Delete	Del			
		Select All Find Find Next	Ctrl+A Ctrl+F F3			
		Add Nodes Add Nodes with Plug-In Plug-In Options	•			
		Locate	•	•		
🔊 Data 🖉	Setup	Group Ungroup Rename				
Hierarchy Disp	Hierarchy Display: ····· ☑ ● NewCLKD∨dr	Mnemonic Table Setup			×	Data Log: 🛃
-		Create SignalTap II List	File			signal_set
		Invert Signal Align Left • Align Right				
auto signa	altan 0	MSB on Top, LSB on Bot LSB on Top, MSB on Bot	tom tom			
		Bus Display Format	•			