Figure 2–1. Cyclone II EP2C20 Device Block Diagram

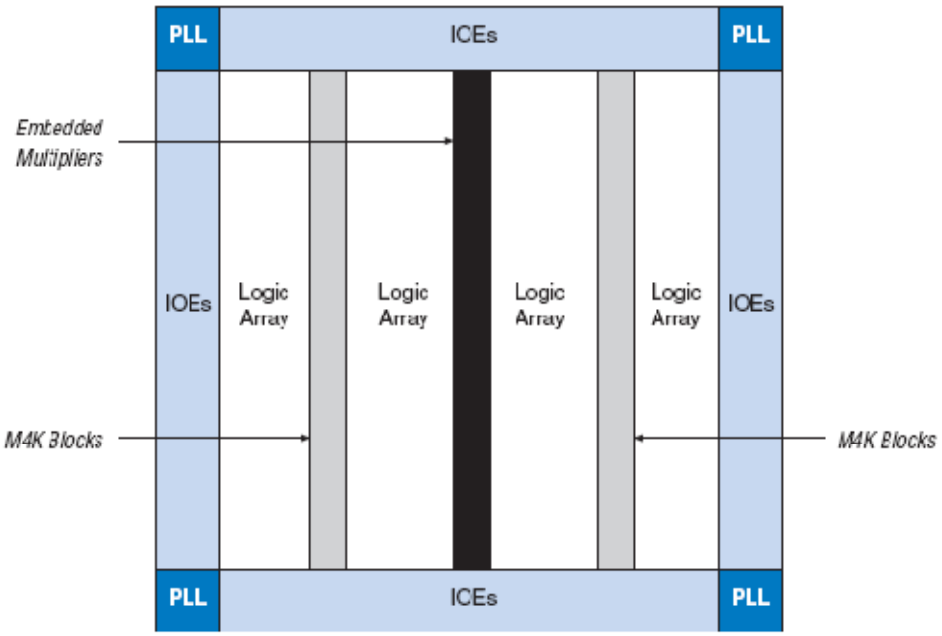


Figure 2–2. Cyclone II LE

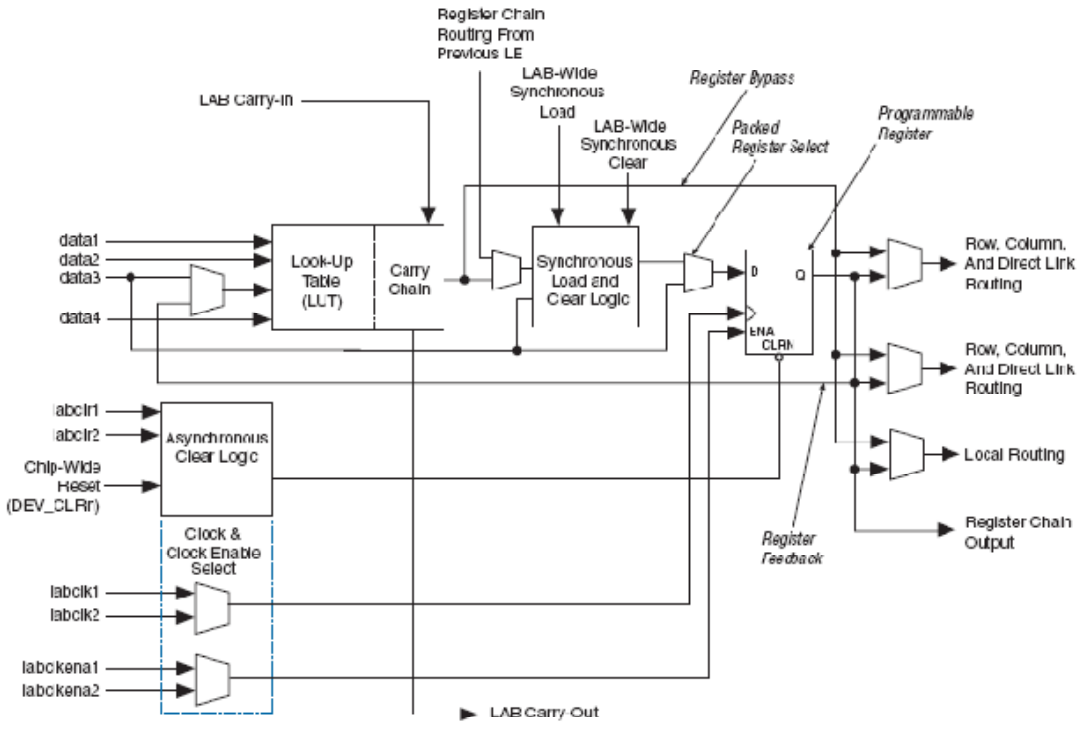


Figure 2–3. LE in Normal Mode

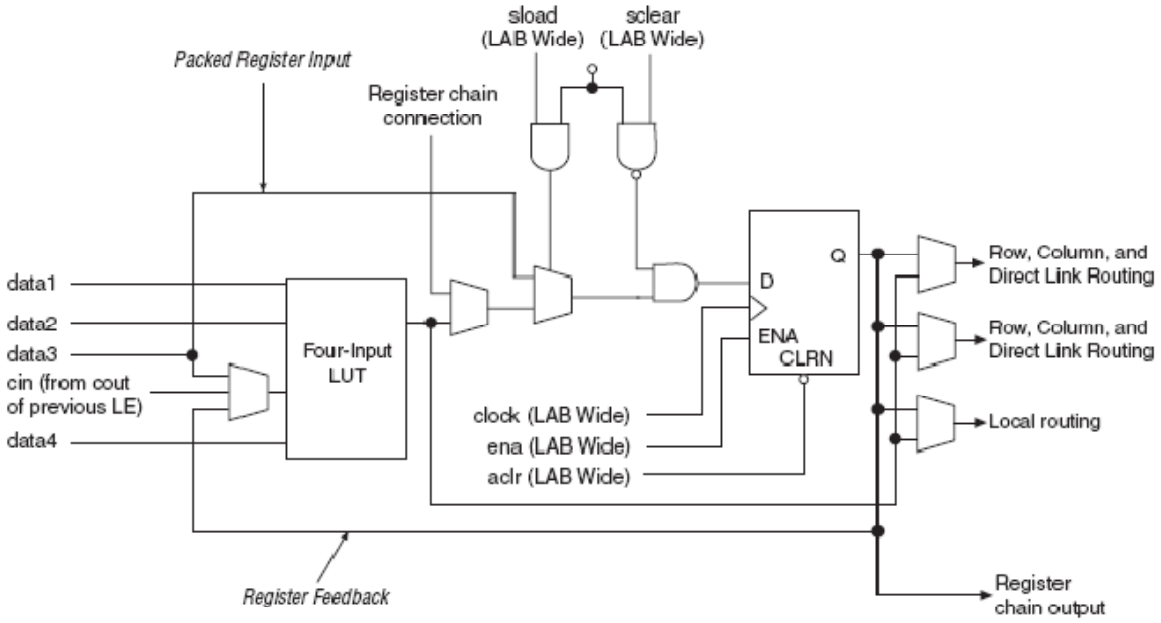


Figure 2–4. LE in Arithmetic Mode

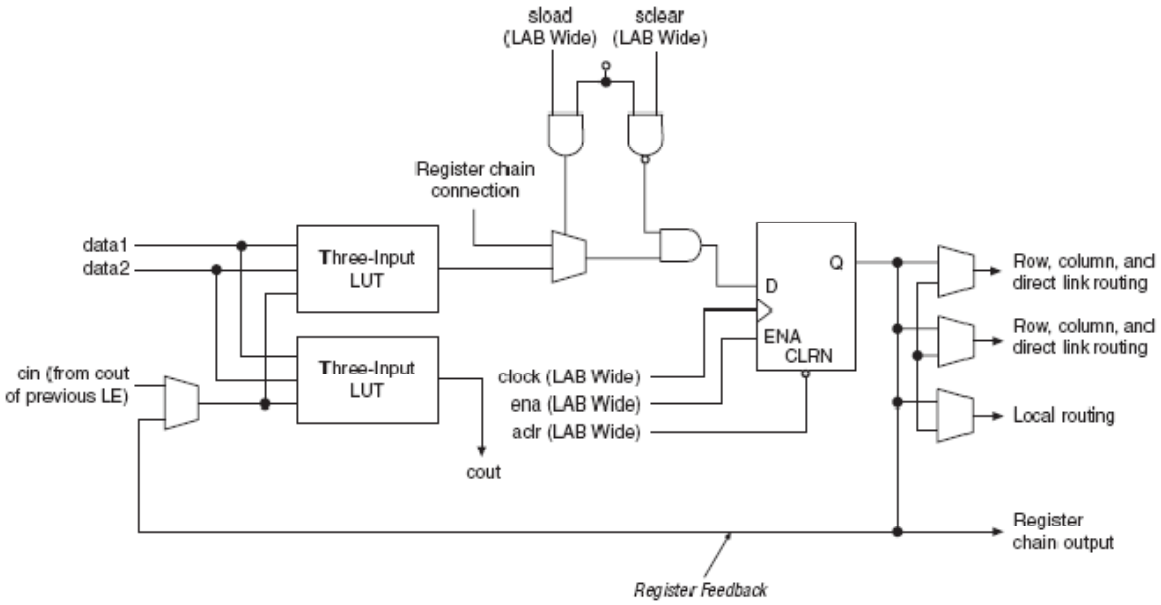


Figure 2–5. Cyclone II LAB Structure

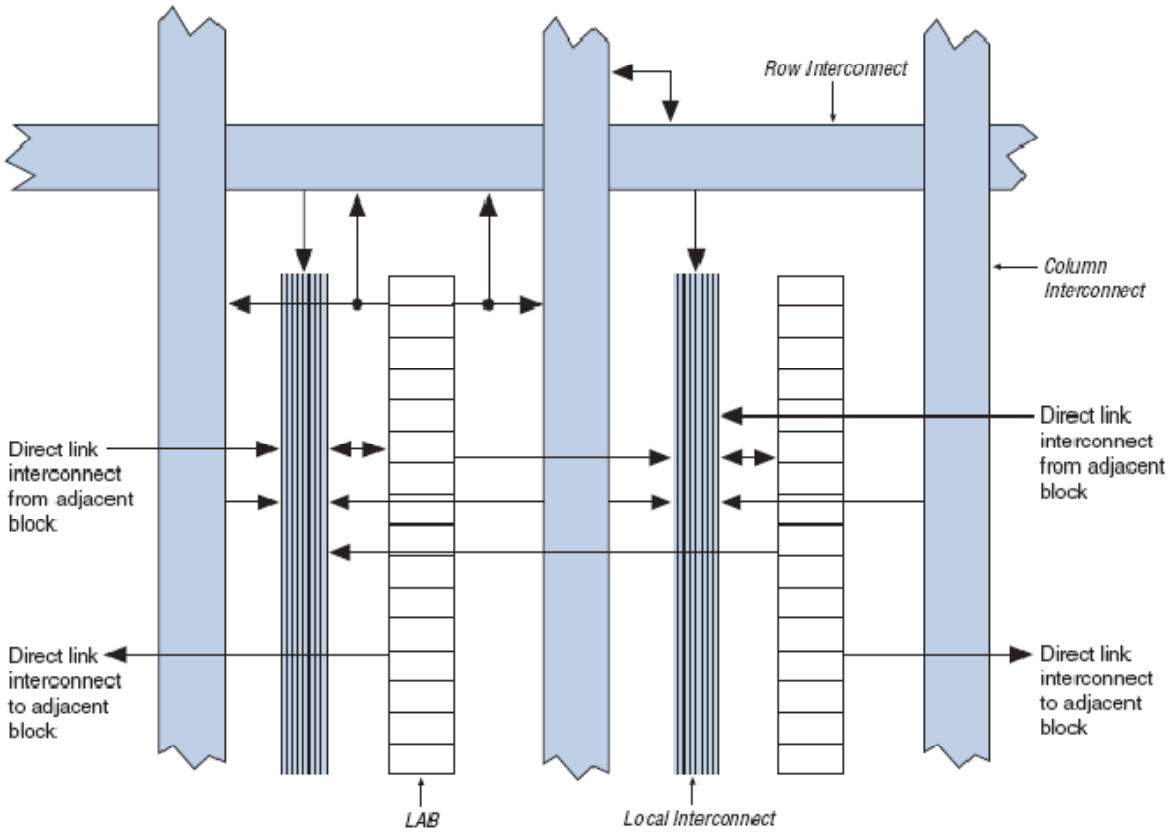


Figure 2–6. Direct Link Connection

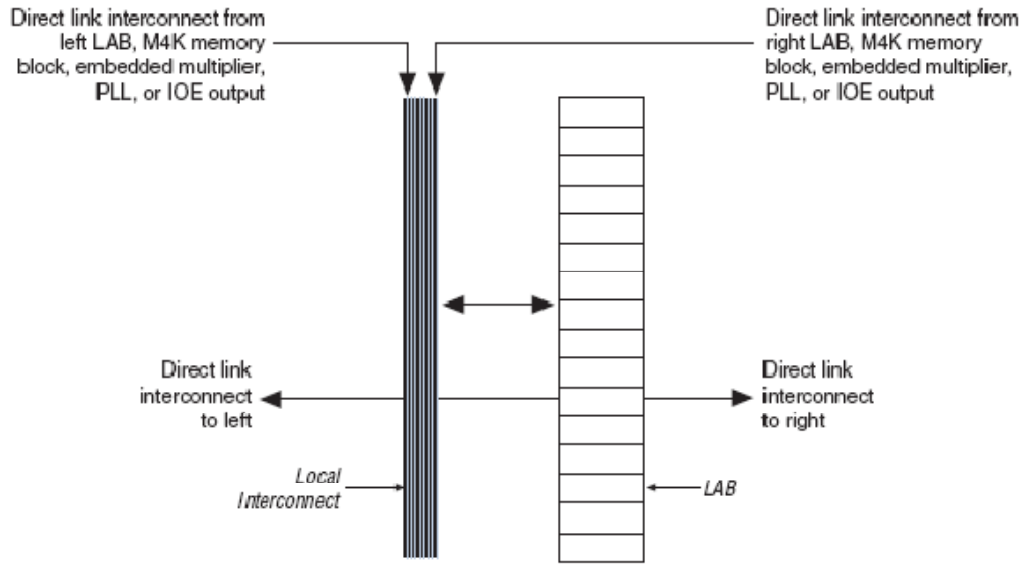


Figure 2–7. LAB-Wide Control Signals

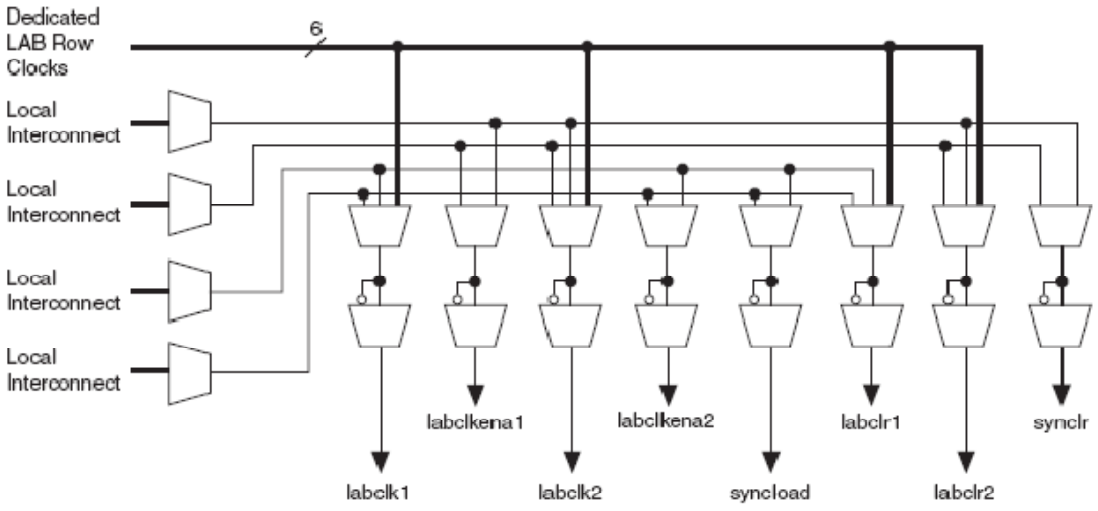
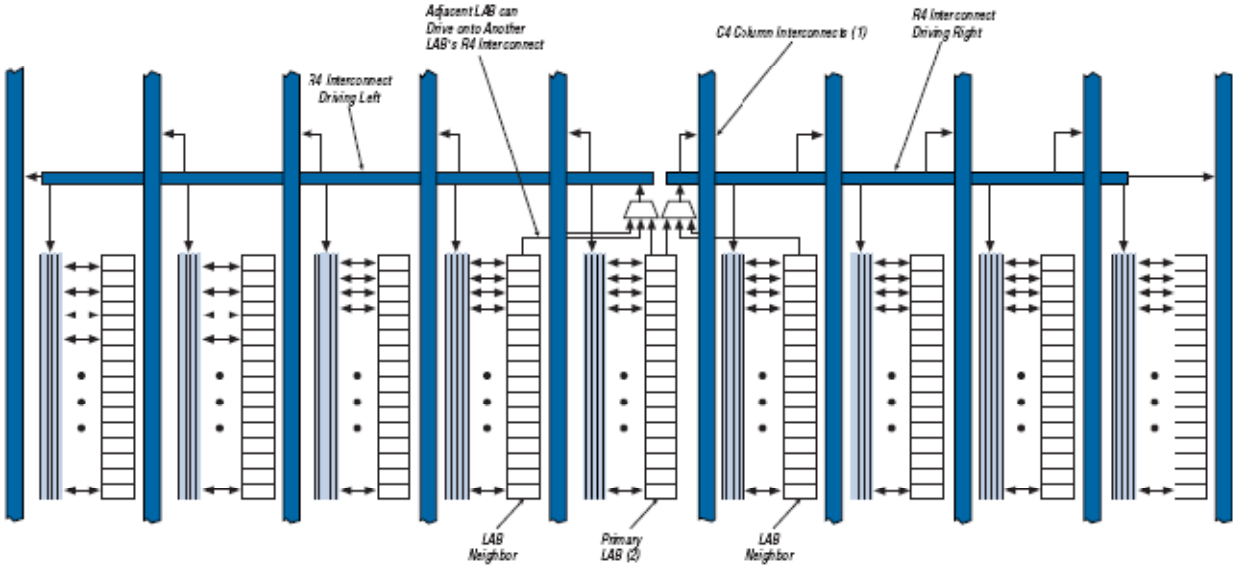


Figure 2–8. R4 Interconnect Connections



Notes to Figure 2–8:

(1) C4 interconnects can drive R4 interconnects.

(2) This pattern is repeated for every LAB in the LAB row.

Figure 2–9. Register Chain Interconnects

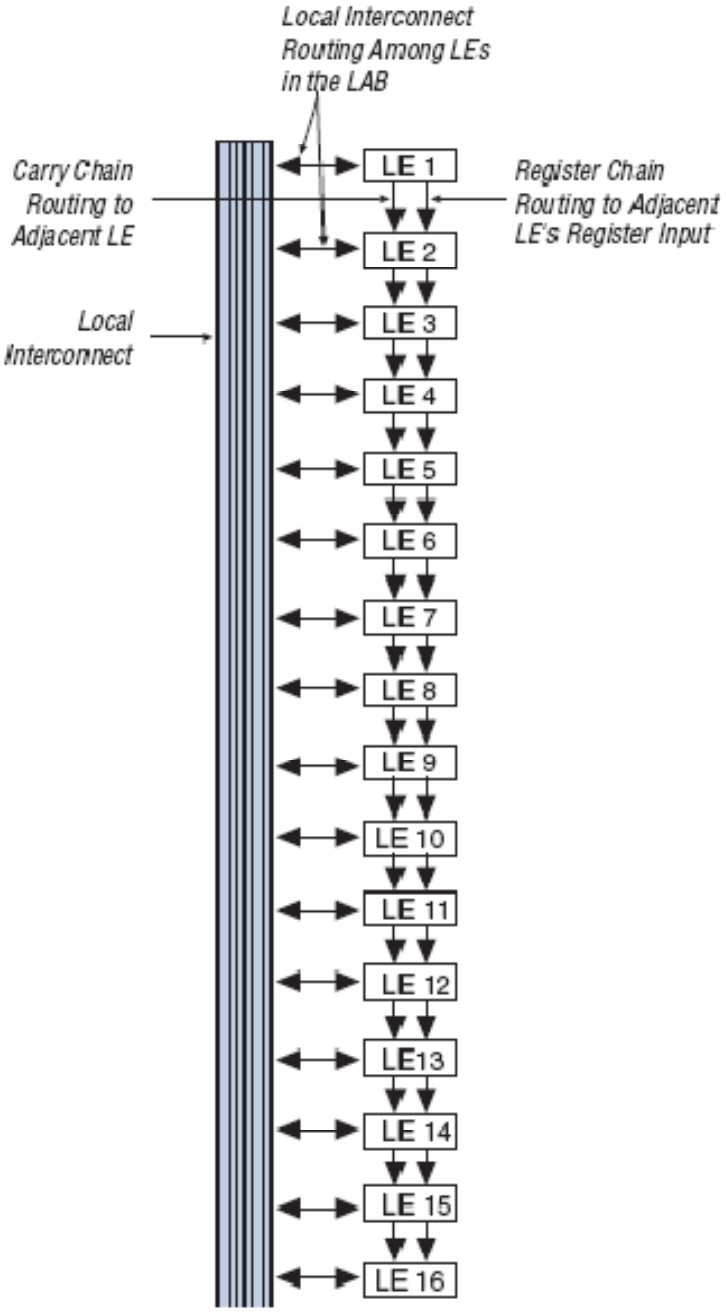
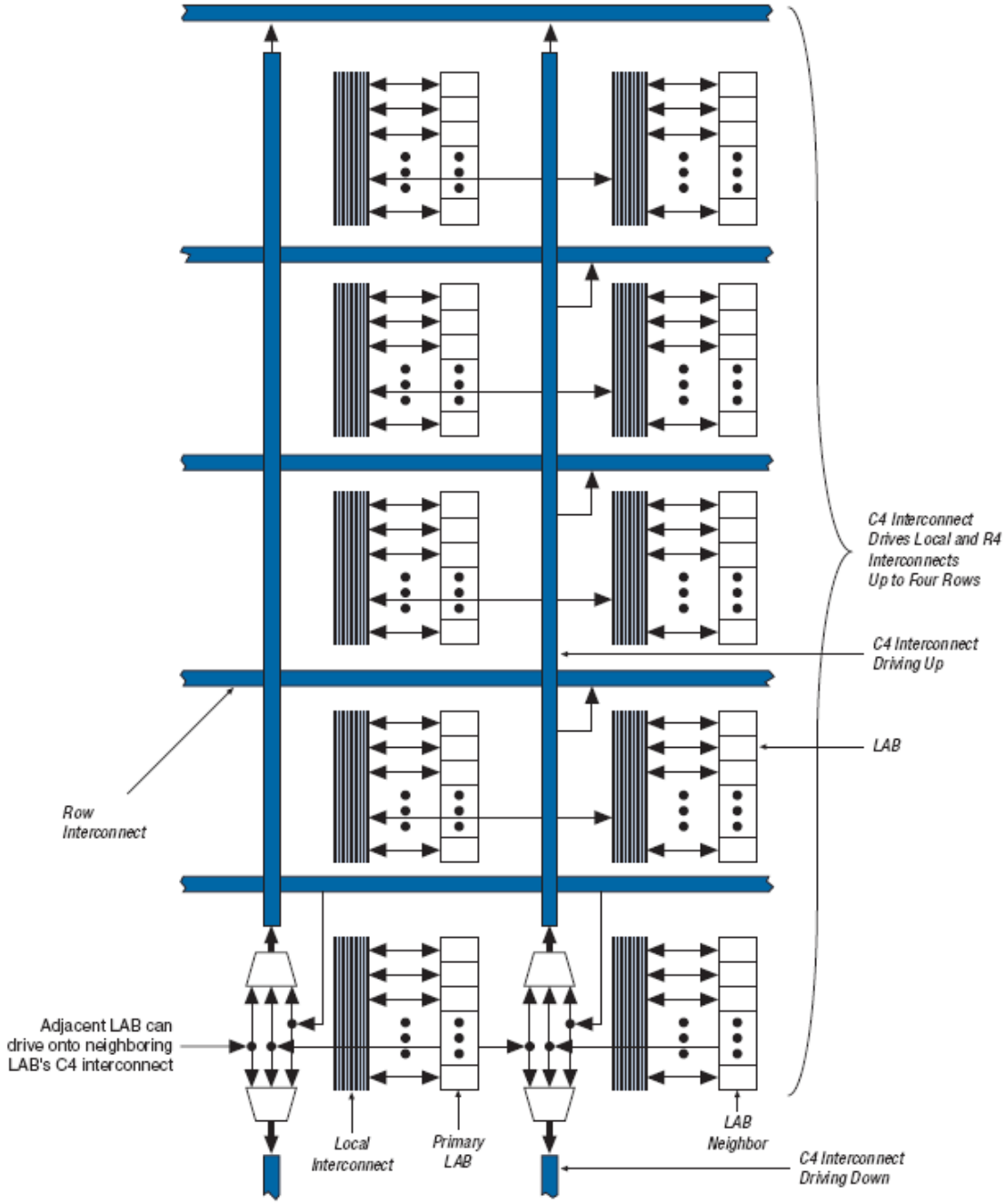


Figure 2–10. C4 Interconnect Connections *Note (1)*



Note to Figure 2–10:

(1) Each C4 interconnect can drive either up or down four rows.

Figure 2–17. M4K RAM Block LAB Row Interface

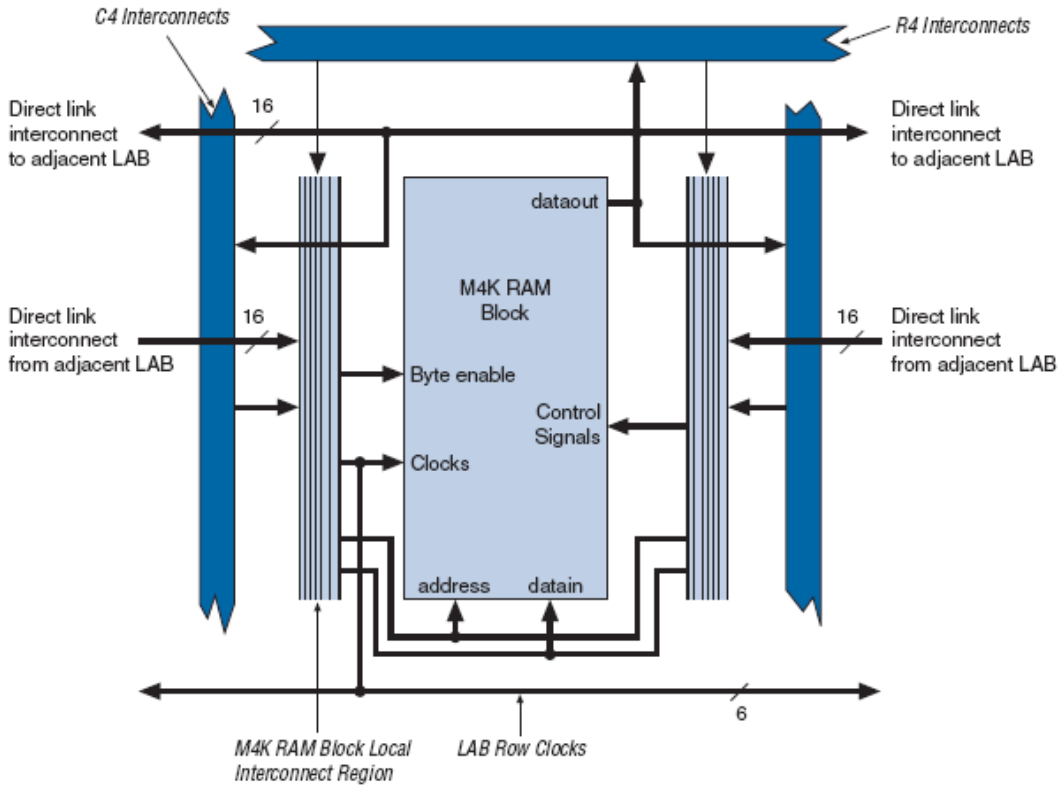
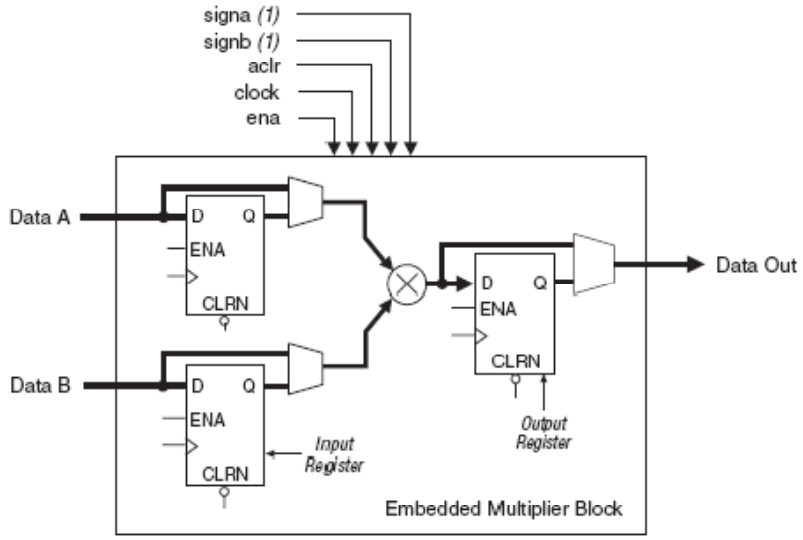


Figure 2–18. Multiplier Block Architecture



Note to Figure 2–18:
(1) If necessary, these signals can be registered once to match the data signal path.

Figure 2–19. Embedded Multiplier LAB Row Interface

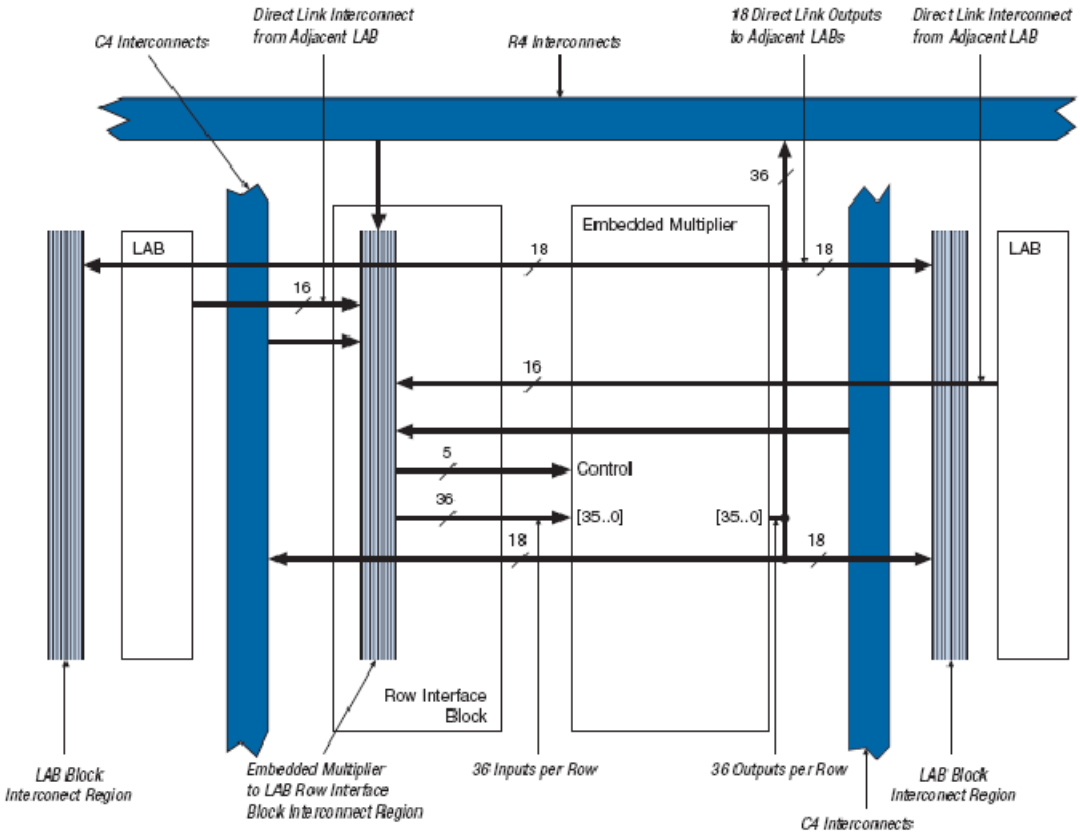
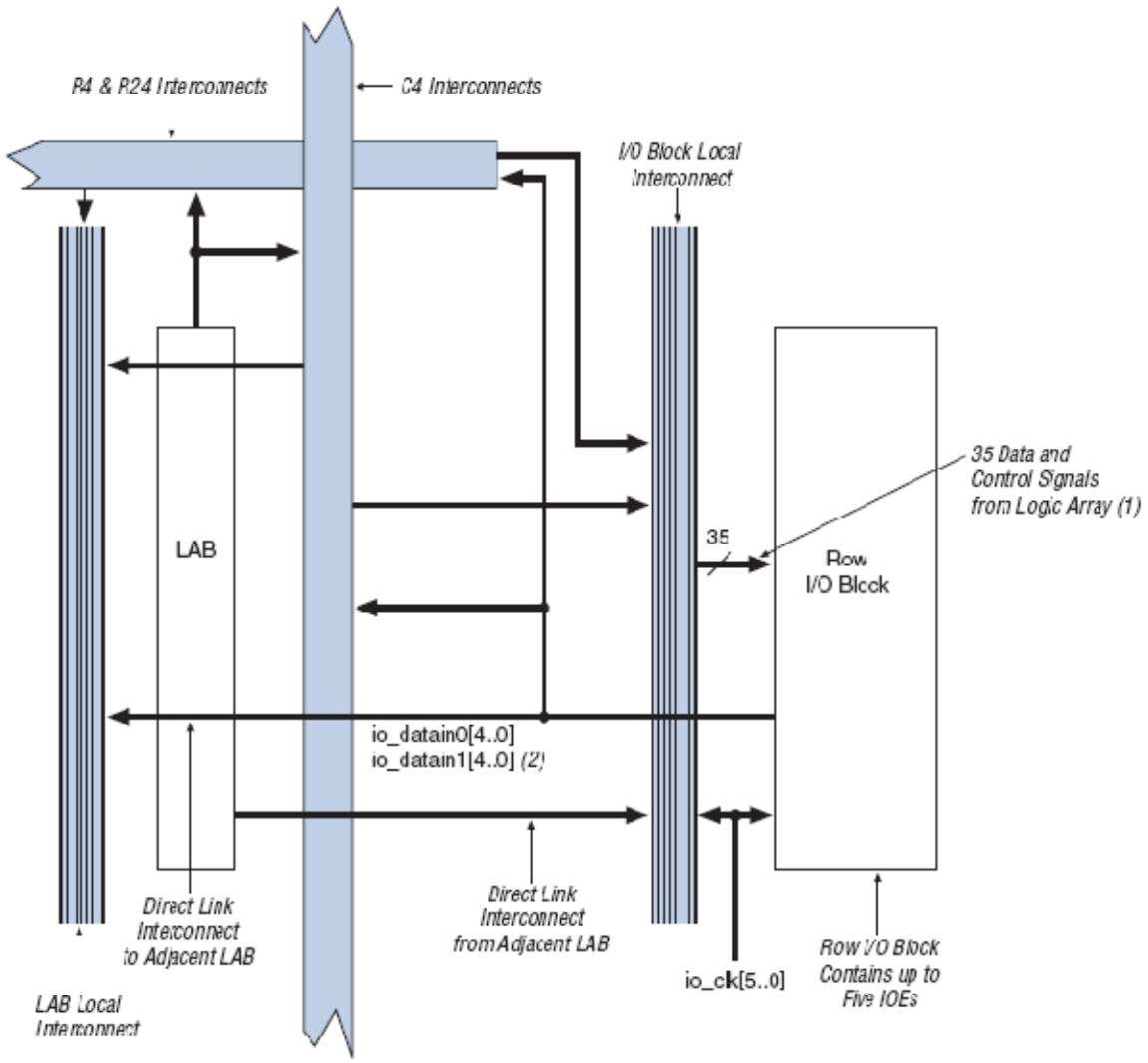


Figure 2–21. Row I/O Block Connection to the Interconnect

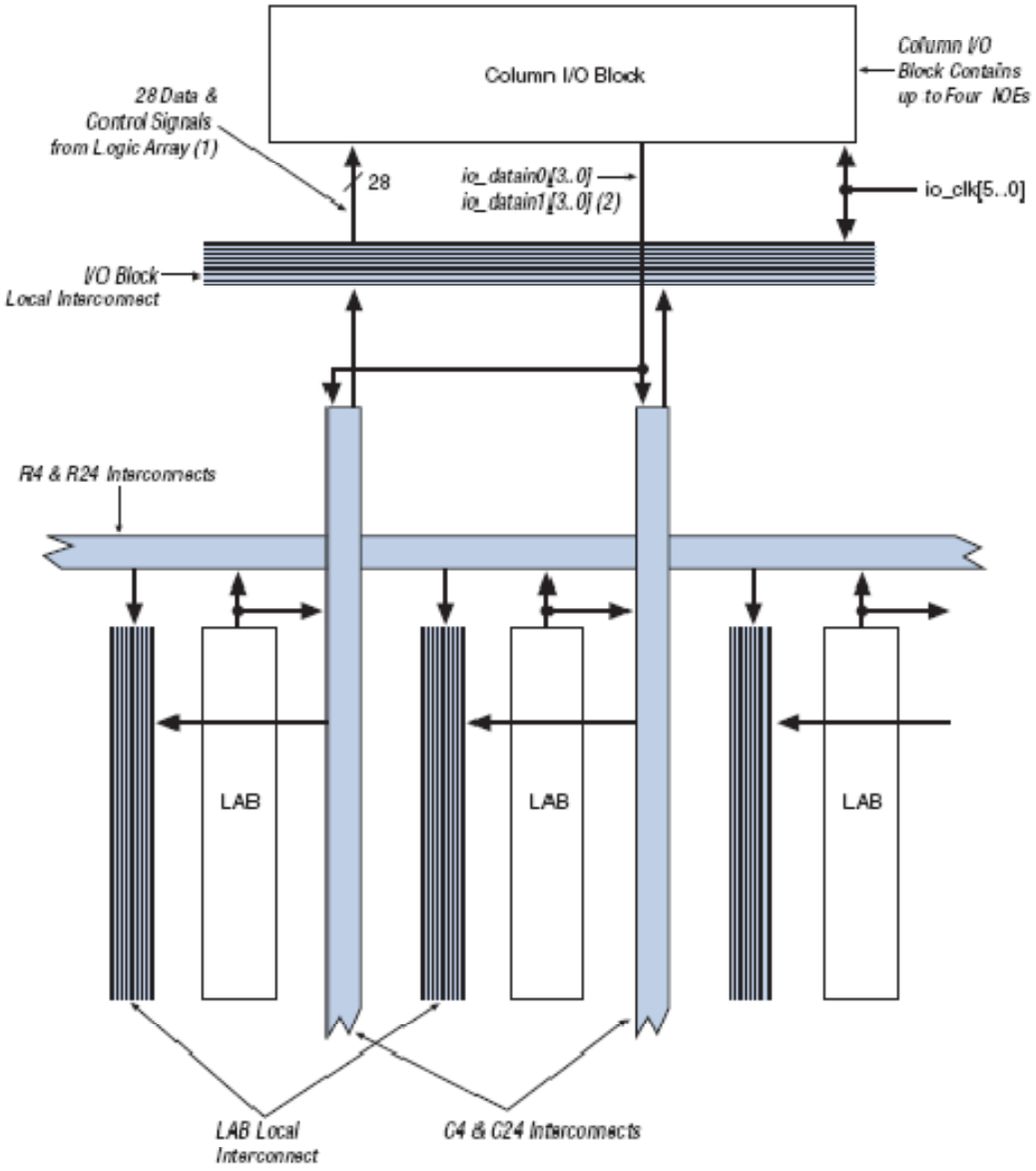


Notes to Figure 2–21:

(1) The 35 data and control signals consist of five data out lines, `io_dataout[4..0]`, five output enables, `io_coe[4..0]`, five input clock enables, `io_cce_in[4..0]`, five output clock enables, `io_cce_out[4..0]`, five clocks, `io_cclk[4..0]`, five asynchronous clear signals, `io_caclr[4..0]`, and five synchronous clear signals, `io_csclr[4..0]`.

(2) Each of the five IOEs in the row I/O block can have two `io_datain` (combinational or registered) inputs.

Figure 2–22. Column I/O Block Connection to the Interconnect



Notes to Figure 2–22:

(1) The 28 data and control signals consist of four data out lines, `io_dataout[3..0]`, four output enables, `io_coe[3..0]`, four input clock enables, `io_cce_in[3..0]`, four output clock enables, `io_cce_out[3..0]`, four clocks, `io_cclk[3..0]`, four asynchronous clear signals, `io_caclr[3..0]`, and four synchronous clear signals, `io_csclr[3..0]`.

(2) Each of the four IOEs in the column I/O block can have two `io_datain` (combinational or registered) inputs.