

Lab 5: Finite State Machines + Datapaths (GCD Calculator)

EEL 4712 – Spring 2010

Objective:

The objective of this lab is to use a finite state machine integrated with a datapath to calculate the greatest common divisor (GCD) of two numbers, using several different VHDL models.

Required tools and parts:

Quartus2, ModelSim-Altera Starter Edition, UF-4712 board

Pre-requisite:

You must be “up-to-speed” with Quartus, Timing Analyzer, ModelSim, and the board before coming to lab.

Pre-lab requirements:

1. Study the following pseudo-code to make sure you understand the basic algorithm for calculating the GCD of two numbers. The code has 2 inputs (X and Y), and one output (*output*).

```
tmpX = X;
tmpY = Y;
while (tmpX != tmpY) {
    if (tmpX < tmpY)
        tmpY = tmpY - tmpX;
    else
        tmpX = tmpX - tmpY;
}
output = tmpX;
```

FSMD

2. Use the provided GCD entity (gcd.vhd), create a custom circuit that implements the GCD algorithm by using the 1-process FSMD model. **This specification must appear in the GCD architecture entitled FSMD.** The entity has a *go* input and *done* output (**revised 2/23**) that work as follows. After being reset, the circuit should wait until *go* becomes 1 (active high), at which point the GCD algorithm should be performed for the given x and y inputs. Upon completion, *done* should be asserted (active high). **Done should remain asserted until the application is started again, which is represented by a 0 on the *go* signal followed by a 1. In other words, the circuit shouldn't continuously execute if *go* is left at 1.**

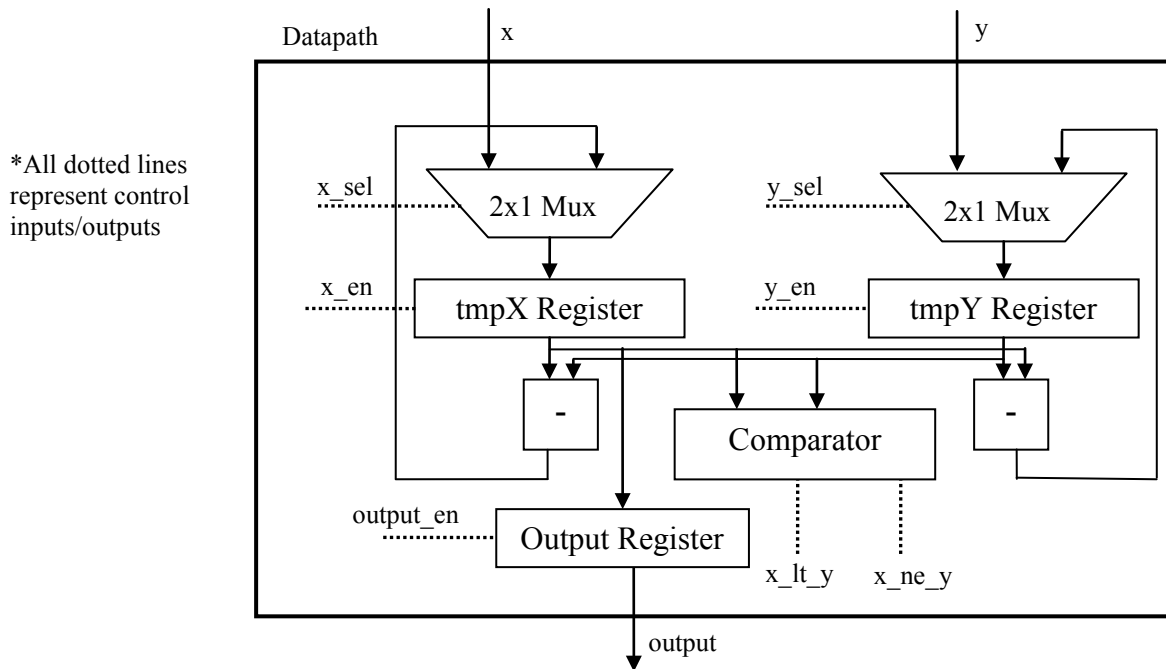
Use the provided testbench (gcd_tb.vhd) to test your architecture. Note that the testbench uses a configuration to specify which gcd architecture is used. **When testing the FSMD, make sure the configuration specifies the FSMD architecture. Also, when simulating, making sure to select the configuration TB_CONFIG, and not the actual testbench.**

FSM+D 1

3. In this step, you will implement a custom circuit that implements the GCD algorithm by using the datapath shown below:

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Implement the datapath by creating an entity `datapath1` (store it in `datapath1.vhd`). You must use a structural description that instantiates all of the components shown. Therefore, you will also need a register entity, a 2x1 mux entity, a subtractor entity, and a comparator entity. The register entity must have an enable input that allows/prevents data from being stored. The comparator entity must have a less than output, which connects to the `x_lt_y` signal, and a not equal output, which connects to the `x_ne_y` signal. You are free to implement these entities however you like, as long as they have these basic capabilities, and as long as each entity uses a generic for the width.

Next, implement a controller entity called `ctrl1` (store it in `ctrl1.vhd`) that uses the control signals for the illustrated datapath to execute the GCD algorithm. Feel free to use either the 1-process or 2-process FSM model (I recommend the 2-process model).

For the provided `gcd` entity implement the structural architecture (`FSM_D1`) that connects the controller to the datapath. You must use the `FSM_D1` architecture.

Use the provided testbench (`gcd_tb.vhd`) to test your architecture. Note that the testbench uses a configuration to specify which `gcd` architecture is used. **When testing the `FSM_D1`, make sure the configuration specifies the `FSM_D1` architecture. Also, when simulating, making sure to select the configuration `TB_CONFIG`, and not the actual testbench.**

FSM+D 2

4. In this step, you will first create a different datapath for the GCD algorithm that only uses a single subtractor. Add any components and/or control signals that are necessary. Call the datapath entity `datapath2` and store it in `datapath2.vhd`. You must use a structural architecture.

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Next, implement a revised controller entity called `ctrl2` (store it in `ctrl2.vhd`) that is based on the revised datapath. Add any control I/O that is required.

For the provided `gcd` entity implement the structural architecture (`FSM_D2`) that connects the controller to the datapath. You must use the `FSM_D2` architecture.

Use the provided testbench (`gcd_tb.vhd`) to test your architecture. Note that the testbench uses a configuration to specify which `gcd` architecture is used. **When testing the `FSM_D2`, make sure the configuration specifies the `FSM_D2` architecture. Also, when simulating, making sure to select the configuration `TB_CONFIG`, and not the actual testbench.**

Top Level

5. Create your own top-level entity `top_level`, stored in `top_level.vhd`, that instantiates one of the `gcd` entities (with a width of 8 bits) such that the `x` and `y` inputs are mapped onto the dip switches, `go` is mapped onto a button, the output is mapped onto the 2 7-segment LEDs (each LED gets 4 bits of the output), and the `done` signal is mapped onto the decimal point. Make sure to add the 7-segment decoder code to your project. To select a particular architecture for the GCD component, you will need to use a configuration. See the provided testbench and the `top_level` entity from lab 3 for examples.

Extra Credit

6. Create a new FSMD (not an FSM+D) architecture for the GCD entity that uses a 2-process model (`gcd_fsmd2.vhd`). Note that I have not shown how to do this. The 2-process FSMD is trickier than the 2-process FSM model and the 1-process FSMD model. You will likely run into issues that will test your understanding of VHDL. However, unlike the 1-process FSMD, the 2-process FSMD model has the advantage of not requiring registers on all outputs. Be sure to inform your TA (or myself) if you are able to get this working.

Implement the new FSMD in the `FSMD2` architecture for the provided GCD entity.

Use the provided testbench (`gcd_tb.vhd`) to test your architecture. Note that the testbench uses a configuration to specify which `gcd` architecture is used. **When testing the `FSMD2`, make sure the configuration specifies the `FSMD2` architecture. Also, when simulating, making sure to select the configuration `TB_CONFIG`, and not the actual testbench.**

Turn in all VHDL. For Step 4, create and submit a diagram illustrating the structure of your revised datapath. There must be only one subtractor.

In-lab procedure (*do as much as possible ahead of time*):

1. Using Quartus, assign pins to each of the `top_level.vhd` inputs/outputs such that the signals are connected to the appropriate locations on the board.
2. Download your design to the board, and test it for different inputs and outputs. Demonstrate the correct functionality for the TA. Make note of the area requirements for the current architecture.
3. Demonstrate the other architectures (`FSMD`, `FSM_D1`, `FSM_D2`, `FSMD2`) to the TA, showing how the area changes. Alternatively, if you do not finish this step, see the lab report section. Note that `FSMD2` is extra credit.

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4. Be prepared to answer simple questions or to make simple extensions that your TA may request. If you have done the pre-lab exercises, these questions should not be difficult.

Lab report: (In-lab part only)

- If you had any problems with portions of the lab that could not be resolved during lab, please discuss them along with possible justifications and solutions. Also, if you did not demo all implementations for your TA, create a table that shows how the area requirements differ for each implementation. *If you had no problems and demoed all parts during lab, this report is not necessary.*

If needed, turn the lab report in on e-learning. Make sure to turn it in to the “lab” section and not the “pre-lab” section.
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