Lab 1: Introduction to EEL 4712 Digital Design Lab

EEL 4712 – Spring 2010

Objective:

The objective of this lab is to introduce the software and hardware development tools to be used in EEL 4712 to design, construct, and test digital circuits. In particular, you will review the use of the Quartus2 software package from Altera for the specification, synthesis, simulation, and testing of a digital design. An 8-bit counter, a 1-bit full-adder, and a 4-bit ripple-carry adder will be designed and simulated in Quartus2. Also, you will also be introduced to the use of the UF-4712 board and to learn the techniques of using an oscilloscope and logic state analyzer (LSA) to test a constructed digital circuit.

Required tools and parts:

Quartus2 software package, UF-4712 board, oscilloscope, logic state analyzer (LSA).

Pre-requisite:

You must be "up-to-speed" with Quartus before coming to lab. Perform Tutorials 1 and 3 (Appendices B and D) in the textbook if necessary. Also, download and read the UF-4712 documents before coming to lab.

Pre-lab requirements:

1. Read the following documents before you come into the lab:
   - Tutorials for LSA and oscilloscope
   - Tutorial for SignalTap II Logic Analyzer
   - UF-4712 Board documents
2. Schematic capture and simulate an 8-bit counter.

   Use the Quartus2 graphical editor to create a .bdf file that contains the design of an 8-bit, synchronous, binary counter that functions as exactly like a 74163 counter. The only exception is the 8-bit counter only has one enable input EN. So, the functions for the 8-bit counter are as follows:

CLR	LD	EN	Function
True	Don't care	Don't care	synchronous CLEAR
False	True	Don't care	synchronous LOAD
False	False	True	Count up
False	False	False	Hold

   - Just as the 74163, the 8-bit counter has a ripple-carry output (RCO).
   - You are to use two 74163 counters (from the "others/maxplus2" library), an AND gate, and the appropriate input and output connectors.

- Perform a **functional** simulation for the circuit. Display all inputs and outputs. Show that the CLR, LD, and EN signals work. Then, allow the counter to count up continuously (for a full 8-bit cycle) to show that it counts up correctly and the RCO output works.
  Note: you do not have to print out the full 8-bit cycle for your report, only some representative samples.
- Set the compiler options as follows. From the "Assignments/device…" command, choose select the device "Cyclone II – EP2C8T144C8".
- Now compile the counter circuit and perform a **timing** simulation.

Turn in on e-learning: the design of the 8-bit counter (.bdf file), functional simulation results, and timing simulation results. Note that the printout of your simulation does not have to be exhaustive. But, you should design your printout such it can convince your TA to give you full credit. Most importantly, the simulation outputs ***must be annotated***.

3. Design and simulate a 4-bit ripple-carry adder: **schematic capture.**
   - Use the Quartus2 graphical editor to create a .bdf file containing a 1-bit full-adder (FA) by connecting the appropriate logic gates.
   - Compile the FA circuit and perform a **timing** simulation for the FA circuit, testing all combinations of the inputs.
   - Use the Quartus2 graphical editor to create a 4-bit ripple-carry adder, using the 1-bit FA as a component. To do this, you will need to convert the FA .bdf file to a symbol file (File->Create/Update->Create Symbol Files). You can then use the FA symbol file in the 4-bit ripple carry .bdf file.
   - Compile and perform **timing** simulation for the 4-bit adder. Note that you do not have to print out the simulation result of all possible combinations of the inputs, only some representative samples.

   Turn in on e-learning: the design of the 4-bit adder (both .bdf files) and all simulation results. Again, the printout of your simulation does not have to be exhaustive. But, you should design your printout so it can convince your TA to give you full credit. Most importantly, the simulation outputs ***must be annotated***.

4. Design and simulate a 4-bit ripple-carry adder: **VHDL specification.**
   - Repeat all the steps of Pre-lab requirement (3) above, except using VHDL. Create two entities: a 1-bit FA, and a 4-bit ripple carry adder. For the 1-bit FA, use one of the behavioral models for combinational logic that was discussed in class. For the 4-bit ripple carry, create a structural architecture using *PORT MAP* statements that combine the 1-bit FA into a 4-bit ripple carry adder.

   Turn in on e-learning: the design of the 4-bit adder (VHDL files) and all ***annotated*** timing simulation results.

In-lab procedure:

1. The TA will give you a demonstration of
   - the use of the oscilloscope to test the counter
   - the use of the LSA to test the counter
   - the use of the SignalTap II LSA
2. Using Quartus, assign pins and download the 8-bit counter from Pre-lab Part 1 to your UF-4712 board.
3. Perform the LSA tutorial, based on the 8-bit counter that you have downloaded in Task 2. Make the specified printouts to be included in your report. Demonstrate to your TA your knowledge of the LSA.
4. Based on the *Tutorial for SignalTap II Logic Analyzer*, use the SignalTap II tool from Quartus to obtain a waveform display of your 8-bit counter.
5. Perform the oscilloscope tutorial. Make the specified printouts to be included in your report. Demonstrate to your TA your knowledge of the oscilloscope. Note, if you have a digital camera, you should bring it to take a snapshot of the oscilloscope display. Otherwise, you have to sketch the oscilloscope outputs by hand.

Lab report: (In-lab part only)

- The lab report must be prepared using a word processor and drawing tool. Make every effort (e.g., spell-check and grammar-check) to produce a neat, readable, and professional document.

- Make sure you give a detailed description of what actions you performed in-lab (i.e. procedures) and included the specified printouts.
- If you had any problems with portions of the lab that could not be resolved during lab, please discuss them along with possible justifications and solutions.

Turn the lab report in on e-learning. Make sure to turn it in to the "lab" section and not the "pre-lab" section.