Lab 1: Fibonacci Calculator

EEL 5721/4720 – Reconfigurable Computing

Objective:

The objective of this lab is to create an FSMD and FSM+D that calculates Fibonacci numbers. It is also your responsibility to build your own testbench.

Required tools and parts:

Vivado, ModelSim-Altera Starter Edition (or equivalent simulator)

Lab requirements:

1. For this lab, the entity we will be creating is a Fibonacci calculator. First, study the following pseudo-code to make sure you understand the basic algorithm. This code assume that the first Fibonacci number corresponds to an *n* value of 0. E.g. fib(0) = 0, fib(1) = 1, fib(2) = 1, fib(3) = 2, etc.

```
// Inputs: go, n
// Outputs: output, done

// Reset values (add any others that you might need)
output = 0; done = 0;

while(1){

   // Wait for go to start circuit
   while (go == 0);
   done = 0;

   // Register the n input (should happen in the cycle go is asserted)
   n_r = n;

   // Initialization
   x_r = 0;
   y_r = 1;

   // Main algorithm
   if (n == 0)
         output = x_r;
   else {
         for (int i=2; i <= n_r; i++) {
               int temp = x_r + y_r;
               x_r = y_r;
               y_r = temp;
         }

         output = y_r;
   }

   // should remained asserted until circuit is started again
   done = 1;
}
```

2. IMPORTANT: The design has the following timing requirements:
   - Done should be cleared 1 cycle after the assertion of go.
   - Upon completion, done should remain asserted indefinitely until go is asserted again.

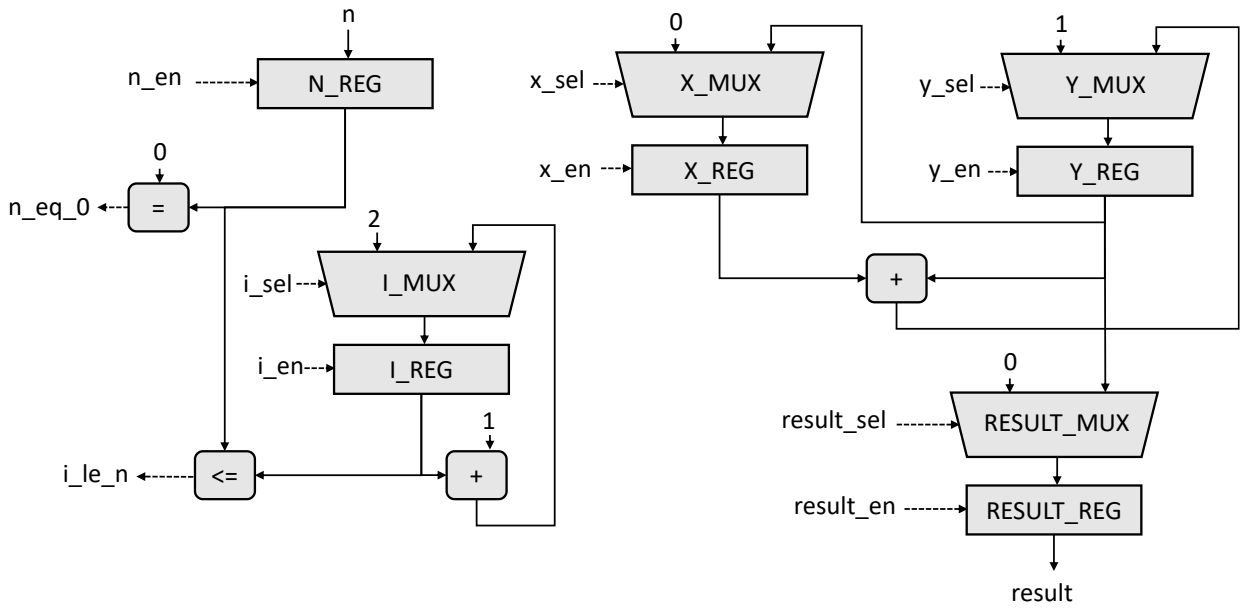
FSMD

3. Create a 1-process FSMD that implements the code shown above. Add the code to the fsmd architecture within fib.vhd.

4. Synthesize your FSMD in Vivado (for any FPGA) and take a screenshot showing no synthesis warnings. ***Make sure that the default_arch architecture of fib.vhd is using the fsmd architecture. Save the screenshot to synthesis_fsmd.jpg***.

FSM+D

5. Create the following datapath by filling in the datapath.vhd file. You can create the datapath structurally or behaviorally, but it must synthesize to this same structure. ***If you create a structural architecture, make sure to add your extra entities to datapath.vhd to ensure that all submissions have the same files.***



6. Create a 2-process FSM controller that controls the datapath from the previous step to implement the required functionality from the pseudo-code in part 1. Your controller should be implemented in the fsm.vhd file.

7. Fill in the fsm_plus_d architecture in fib.vhd to instantiate and connect the datapath and controller.

8. Synthesize your FSM+D in Vivado (for any FPGA) and take a screenshot showing no synthesis warnings. ***Make sure that the default_arch architecture of fib.vhd is using the fsm_plus_d architecture. Save the screenshot to synthesis_fsmd.jpg***.

9. Important: you will likely get these warnings (or something similar) for the FSM+D. These warnings are fine, but only if they occur at time 0. They are caused by a value that isn't '0' or '1' reaching an arithmetic operation. This is often unavoidable at time 0 because certain signals haven't been initialized yet depending on how the simulation orders the execution of processes.

*# ** Warning: NUMERIC_STD."<=": metavalue detected, returning FALSE*
 # Time: 0 ns Iteration: 0 Instance: /fib_tb/DUT/U_FIB/U_DATAPATH

*# ** Warning: NUMERIC_STD."=": metavalue detected, returning FALSE*
 # Time: 0 ns Iteration: 0 Instance: /fib_tb/DUT/U_FIB/U_DATAPATH

Testbench

10. Create a testbench in fib_tb.vhd that tests at least 3 different values of *n*. You are only required to test the range 0 <= *n* <= 47. I would highly suggest testing all the input values to ensure that your design is working. I will be testing it with a very thorough testbench, which will likely catch errors your testbench might miss.

11. Your testbench should be used to test both the fsmd and fsm_plus_d architectures. You can do this either by manually changing the architecture that is used in the testbench, or by changing the default_arch architecture in fib.vhd. For this lab, do *not* create multiple testbench files.

12. Take a screenshot of your testbench running the FSMD and save it to a file testbench_fsmd.jpg.

13. Take a screenshot of your testbench running the FSM+D and save it to a file testbench_fsm_plus_d.jpg.

14. An additional testbench is provided in fib_crv_tb.vhd that uses a strategy called constrained-random verification. It performs numerous random tests, while also verifying the timing of the done signal. I would highly recommend using it in addition to your own testbench because the graders will use something similar.

Turn in instructions:

Submit the following to Canvas as a single zip file where the file name is your UFID. e.g., for 12345678 your submission should be a single zip called 12345678.zip. Do not include any extra folders, do not change the name of any files, do not use another compression format, etc. This specific structure is intended to help automate grading.

- fib.vhd
- fsm.vhd
- datapath.vhd
- fib_tb.vhd
- synthesis_fsmd.jpg
- synthesis_fsm_plus_d.jpg
- testbench_fsmd.jpg
- testbench_fsm_plus_d.jpg
- README.txt - If any problems occurred that I should be aware of for grading, include them here.