

# VHDL Tutorial

EEL 4720/5721 – Reconfigurable Computing

## Introduction:

In this lab, you will be implementing and testing some basic digital circuits in VHDL to familiarize yourself with VHDL simulations and synthesis. Before starting, download all provided code off the website, which includes skeleton VHDL files and testbenches for simulations. If you are confused about the how each entity works, use google or look at the testbench code to see the correct output. Make sure to read my provided VHDL tutorial. Instructions for how to simulate and synthesis will be given in class, although I encourage you to figure it out from the ISE documentation.

You will submit this lab on e-learning, but it will not be graded. Instead, in the case of borderline final grades, I will check to see how much effort was made on this lab.

### Part 1 – 2-to-4 Decoder

For part 1, you will be modifying the dec2to4.vhd file. The entity for the decoder has been provided, along with 4 empty architectures. Implement each architecture using the construct suggested by the architecture name (e.g., with select, when else, if, case). Simulate each architecture using the provided testbench dec2to4\_tb.vhd. Ensure that there are no failed assertions. Synthesize your design in Xilinx ISE and ensure that there are no warnings.

### Part 2 – 4-to-2 Priority Encoder

Repeat the steps of part 1 for the 4-to-2 priority encoder (enc4to2.vhd). For this part, you only need two architectures based on the if and the case statement. Assume that higher inputs have priority over lower inputs. The valid output should be asserted when any of the inputs are 1 and should be 0 when all the inputs are 0. This valid bit is needed to understand the output of “00” for an input of “0001” and for an input of “0000”.

### Part 3 – Adder + Register

Repeat the previous steps and create an adder followed by a register (add\_pipe.vhd). As specified in the provided file, you should use a behavioral implementation. Note that the output of the adder is one bit wider than the inputs. In other words, the output should include the carry. Although it shouldn't matter, you can assume the inputs are unsigned.

### Part 4 – Multiplier + Register

Repeat part 3, but replace the adder with a multiplier (mult\_pip.vhd). The output of the multiplier should be twice the width of the inputs.

### Part 5 – Datapath

Implement the following datapath structurally. Use the entities from part 3 and part 4, along with the provided register entity (reg.vhd).

