H100 Series

FPGA Application Accelerators

Products in the H100 Series

PCI-X Mainstream

H101-PCIXM

- HPC solution for optimal price/performance
- PCI-X form factor
- Single Xilinx® Virtex 4 FPGA processor
- SRAM and SDRAM external memory
- Four high-speed serial I/O system links
- Supported by Nallatech's application development flow and ANSI C-to-FPGA compiler
- Ideal for adding FPGA compute capability to new or existing clusters

6.4	20	64
DOUBLE PRECISION GFLOPS SUSTAINED	SINGLE PRECISION GFLOPS SUSTAINED	INT16 GigaOPS SUSTAINED

IBM® EBlade

H102-EBLADE

- IBM® BladeCenter® expansion blade
- Two Xilinx® Virtex 4 FPGA processors
- SRAM and SDRAM external memory
- Eight high-speed serial I/O system links
- Supported by Nallatech's application development flow and ANSI C-to-FPGA compiler
- Ideal for adding FPGA compute capability to IBM® BladeCenter® clusters

12.8	40	128
DOUBLE PRECISION GFLOPS SUSTAINED	SINGLE PRECISION GFLOPS SUSTAINED	INT16 GigaOPS SUSTAINED

IBM® BladeCenter®

H102-BLADECENTER

- IBM® HS21 BladeCenter®
- Single FPGA expansion blade with two Xilinx® Virtex 4 FPGA processors
- Eight high-speed serial I/O system links
- Supported by Nallatech's application development flow and ANSI C-to-FPGA compiler
- The ideal platform for adding FPGA compute capability to IBM® BladeCenter® clusters

12.8	40	128
DOUBLE PRECISION GFLOPS SUSTAINED	SINGLE PRECISION GFLOPS SUSTAINED	INT16 GigaOPS SUSTAINED

IBM® BladeCenter®

H114-BLADECENTER

- Fully loaded IBM® HS21BladeCenter®
- Seven FPGA expansion blades each with two Xilinx® Virtex 4 FPGA processors
- Fifty-six high-speed serial I/O system links
- Supported by Nallatech's application development flow and ANSI C-to-FPGA compiler
- The ideal platform for adding FPGA compute capability to IBM® BladeCenter® clusters

89.6	280	896
DOUBLE PRECISION GFLOPS SUSTAINED	SINGLE PRECISION GFLOPS SUSTAINED	INT16 GigaOPS SUSTAINED

H100 Series

FPGA Application Accelerators

Technical Specification

	H101-PCIXM	H102-EBLADE	H102-BLADECENTER	H114-BLADECENTER
FPGA Compute Engine				
Total number of FPGA Processors	1	2	2	14
Xilinx FPGA Type	Virtex-4 LX100	Virtex-4 LX100	Virtex-4 LX100	Virtex-4 LX100
Internal Memory per FPGA processor	0.5 MBytes RAM distributed across FPGA, 0.5 TBytes/sec bandwidth	0.5 MBytes RAM distributed across FPGA, 0.5 TBytes/sec bandwidth	0.5 MBytes RAM distributed across FPGA, 0.5 TBytes/sec bandwidth	0.5 MBytes RAM distributed across FPGA, 0.5 TBytes/sec bandwidth
External SRAM per FPGA processor	16 MBytes DDR-II SRAM across 4 banks, 6.4GBytes/sec total bandwidth	16 MBytes DDR-II SRAM across 4 banks, 6.4GBytes/sec total bandwidth	16 MBytes DDR-II SRAM across 4 banks, 6.4GBytes/sec total bandwidth	16 MBytes DDR-II SRAM across 4 banks, 6.4GBytes/sec total bandwidth
External SDRAM per FPGA processor	512 MBytes DDR2 SDRAM in 1 bank, 3.2GBytes/sec bandwidth	512 MBytes DDR2 SDRAM in 1 bank, 3.2GBytes/sec bandwidth	512 MBytes DDR2 SDRAM in 1 bank, 3.2GBytes/sec bandwidth	512 MBytes DDR2 SDRAM in 1 bank, 3.2GBytes/sec bandwidth
Max # double precision FPUs	32	64	64	448
Max # single precision FPUs	100	200	200	1,400
Max # INT16 Units	320	640	640	4,480
FPGA clock frequency	200MHz	200MHz	200MHz	200MHz
Inter compute engine serial comms	4x 2.5 Gbit/sec serial links	8x 2.5 Gbit/sec serial links	16x 2.5 Gbit/sec serial links	56x 2.5 Gbit/sec serial links
Serial comms latency	340ns	340ns	340ns	340ns
System Performance				
Double Precision Floating Point	6.4 GigaFLOPS	12.8 GigaFLOPS	12.8 GigaFLOPS	89.6 GigaFLOPS
Single Precision Floating Point	20 GigaFLOPS	40 GigaFLOPS	40 GigaFLOPS	280 GigaFLOPS
Integer 16	64 GigaOPS	128 GigaOPS	128 GigaOPS	896 GigaOPS
Power Consumption				
Total Power Consumption (typical)	25W	50W	150W	500W
Development Tools Support				
Supported Compilers	DIME-C Impulse-C Mitrionics Mitrion-C	DIME-C Impulse-C Mitrionics Mitrion-C	DIME-C Impulse-C Mitrionics Mitrion-C	DIME-C Impulse-C Mitrionics Mitrion-C
Host Configuration				
HS21 Blades	Not Applicable	Not Applicable	Intel Xeon Processor 5110 (1.60GHz, 1066MHz) 2x2MB L2 Cache, Dual Core*	Intel Xeon Processor 5110 (1.60GHz, 1066MHz) 2x2MB L2 Cache, Dual Core*

Actual performance is dependant on the end application and the extent to which the algorithms can be pipelined or parallelized.

Ordering Information

H101 PCI-X Mainstream	H101-PCIXM
H102 BladeCenter expansion blade	H102-EBLADE
H102 BladeCenter Solution: IBM BladeCenter Chassis, H102 blade	H102-BLADECENTER
H114 BladeCenter Solution: IBM BladeCenter Chassis, 7 H102 blades	H114-BLADECENTER
H1XX BladeCenter Solution: IBM BladeCenter Chassis with choice of 4, 6, 8, 10 or 12 FPGAs	H1XX-BLADECENTER (replace XX with the number of FPGAs: 04, 06, 08, 10 or 12)
Nallatech HPC Software Toolkit	H100-DEVKIT-S

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Virtex-4 Family Overview

DS112 (v2.0) January 23, 2007 **Preliminary Product Specification**

General Description

Combining Advanced Silicon Modular Block (ASMBL™) architecture with a wide variety of flexible features, the Virtex™-4 Family from Xilinx greatly enhances programmable logic design capabilities, making it a powerful alternative to ASIC technology. Virtex-4 FPGAs comprise three platform families—LX, FX, and SX—offering multiple feature choices and combinations to address all complex applications. The wide array of Virtex-4 hard-IP core blocks includes the PowerPC™ processors (with a new APU interface), tri-mode Ethernet MACs, 622 Mb/s to 6.5 Gb/s serial transceivers, dedicated DSP slices, high-speed clock management circuitry, and source-synchronous interface blocks. The basic Virtex- 4 building blocks are enhancements of those found in the popular Virtex, Virtex-E, Virtex-II, Virtex-II Pro, and Virtex-II Pro X product families, so previous-generation designs are upward compatible. Virtex-4 devices are produced on a state-of-the-art 90-nm copper process using 300-mm (12-inch) wafer technology..

Summary of Virtex-4 Family Features

- Three Families — LX/SX/FX
  - Virtex-4 LX: High-performance logic applications solution
  - Virtex-4 SX: High-performance solution for digital signal processing (DSP) applications
  - Virtex-4 FX: High-performance, full-featured solution for embedded platform applications
- Xesium™ Clock Technology
  - Digital clock manager (DCM) blocks
  - Additional phase-matched clock dividers (PMCD)
  - Differential global clocks
- XtremeDSP™ Slice
  - 18 x 18, two's complement, signed Multiplier
  - Optional pipeline stages
  - Built-in Accumulator (48-bit) and Adder/Subtracter
- Smart RAM Memory Hierarchy
  - Distributed RAM
  - Dual-port 18-Kbit RAM blocks
    - Optional pipeline stages
    - Optional programmable FIFO logic automatically remaps RAM signals as FIFO signals
  - High-speed memory interface supports DDR and DDR-2 SDRAM, QDR-II, and RLDRAM-II.
- SelectIO™ Technology
  - 1.5V to 3.3V I/O operation
  - Built-in ChipSync™ source-synchronous technology
  - Digitally controlled impedance (DCI) active termination
  - Fine grained I/O banking (configuration in one bank)
- Flexible Logic Resources
- Secure Chip AES Bitstream Encryption
- 90-nm Copper CMOS Process
- 1.2V Core Voltage
- Flip-Chip Packaging including Pb-Free Package Choices
- RocketIO™ 622 Mb/s to 6.5 Gb/s Multi-Gigabit Transceiver (MGT) [*FX only*]
- IBM PowerPC RISC Processor Core [*FX only*]
  - PowerPC 405 (PPC405) Core
  - Auxiliary Processor Unit Interface (User Coprocessor)
- Multiple Tri-Mode Ethernet MACs [*FX only*]

Table 1: **Virtex-4 FPGA Family Members**

Device	Configurable Logic Blocks (CLBs)(1)				XtremeDSP Slices(2)	Block RAM		DCMs	PMCDs	PowerPC Processor Blocks	Ethernet MACs	RocketIO Transceiver Blocks	Total I/O Banks	Max User I/O
	Array(3) Row x Col	Logic Cells	Slices	Max Distributed RAM (Kb)		18 Kb Blocks	Max Block RAM (Kb)							
XC4VLX15	64 x 24	13,824	6,144	96	32	48	864	4	0	N/A	N/A	N/A	9	320
XC4VLX25	96 x 28	24,192	10,752	168	48	72	1,296	8	4	N/A	N/A	N/A	11	448
XC4VLX40	128 x 36	41,472	18,432	288	64	96	1,728	8	4	N/A	N/A	N/A	13	640
XC4VLX60	128 x 52	59,904	26,624	416	64	160	2,880	8	4	N/A	N/A	N/A	13	640
XC4VLX80	160 x 56	80,640	35,840	560	80	200	3,600	12	8	N/A	N/A	N/A	15	768
XC4VLX100	192 x 64	110,592	49,152	768	96	240	4,320	12	8	N/A	N/A	N/A	17	960
XC4VLX160	192 x 88	152,064	67,584	1056	96	288	5,184	12	8	N/A	N/A	N/A	17	960
XC4VLX200	192 x 116	200,448	89,088	1392	96	336	6,048	12	8	N/A	N/A	N/A	17	960

Table 1: **Virtex-4 FPGA Family Members *(Continued)***

Device	Configurable Logic Blocks (CLBs)(1)				XtremeDSP Slices(2)	Block RAM		DCMs	PMCDs	PowerPC Processor Blocks	Ethernet MACs	RocketIO Transceiver Blocks	Total I/O Banks	Max User I/O
	Array(3) Row x Col	Logic Cells	Slices	Max Distributed RAM (Kb)		18 Kb Blocks	Max Block RAM (Kb)							
XC4VSX25	64 x 40	23,040	10,240	160	128	128	2,304	4	0	N/A	N/A	N/A	9	320
XC4VSX35	96 x 40	34,560	15,360	240	192	192	3,456	8	4	N/A	N/A	N/A	11	448
XC4VSX55	128 x 48	55,296	24,576	384	512	320	5,760	8	4	N/A	N/A	N/A	13	640
XC4VFX12	64 x 24	12,312	5,472	86	32	36	648	4	0	1	2	N/A	9	320
XC4VFX20	64 x 36	19,224	8,544	134	32	68	1,224	4	0	1	2	8	9	320
XC4VFX40	96 x 52	41,904	18,624	291	48	144	2,592	8	4	2	4	12	11	448
XC4VFX60	128 x 52	56,880	25,280	395	128	232	4,176	12	8	2	4	16	13	576
XC4VFX100	160 x 68	94,896	42,176	659	160	376	6,768	12	8	2	4	20	15	768
XC4VFX140	192 x 84	142,128	63,168	987	192	552	9,936	20	8	2	4	24	17	896

Notes:
1. One CLB = Four Slices = Maximum of 64 bits.
2. Each XtremeDSP slice contains one 18 x 18 multiplier, an adder, and an accumulator
3. Some of the row/column array is used by the processors in the FX devices.

System Blocks Common to All Virtex-4 Families

Xesium Clock Technology

- Up to twenty Digital Clock Manager (DCM) modules
  - Precision clock deskew and phase shift
  - Flexible frequency synthesis
  - Dual operating modes to ease performance trade-off decisions
  - Improved maximum input/output frequency
  - Improved phase shifting resolution
  - Reduced output jitter
  - Low-power operation
  - Enhanced phase detectors
  - Wide phase shift range
- Companion Phase-Matched Clock Divider (PMCD) blocks
- Differential clocking structure for optimized low-jitter clocking and precise duty cycle
- 32 Global Clock networks
- Regional I/O and Local clocks

Flexible Logic Resources

- Up to 40% speed improvement over previous generation devices
- Up to 200,000 logic cells including:
  - Up to 178,176 internal registers with clock enable (XC4VLX200)
  - Up to 178,176 look-up tables (LUTs)
  - Logic expanding multiplexers and I/O registers
- Cascadable variable shift registers or distributed memory capability

500 MHz XtremeDSP Slices

- Dedicated 18-bit x 18-bit multiplier, multiply-accumulator, or multiply-adder blocks
- Optional pipeline stages for enhanced performance
- Optional 48-bit accumulator for multiply accumulate (MACC) operation
- Integrated adder for complex-multiply or multiply-add operation
- Cascadeable Multiply or MACC
- Up to 100% speed improvement over previous generation devices.

500 MHz Integrated Block Memory

- Up to 10 Mb of integrated block memory
- Optional pipeline stages for higher performance
- Multi-rate FIFO support logic
  - Full and Empty Flag support
  - Fully programmable AF and AE Flags
  - Synchronous/ Asynchronous Operation
- Dual-port architecture
- Independent read and write port width selection (RAM only)
- 18 Kbit blocks (memory and parity/sideband memory support)
- Configurations from 16K x 1 to 512 x 36 (4K x 4 to 512 x 36 for FIFO operation)
- Byte-write capability (connection to PPC405, etc.)
- Dedicated cascade routing to form 32K x 1 memory without using FPGA routing
- Up to 100% speed improvement over previous generation devices.

1.1.2 How DIMEtalk Works Within a Nallatech FPGA Computing System

Figure 1 shows how DIMEtalk abstracts the features of the hardware platform to provide an easy to use development environment for implementing applications on multi-FPGA systems. Standard VHDL design flows are complemented with support for third-party compiler tools alongside an integrated C to VHDL Function Generator, DIME-C, enabling developers to select the design flow most appropriate to their application.

Communications networks between algorithm blocks, memory and I/O interfaces can be rapidly created across multiple FPGAs through the GUI-based application development environment. This functionality enables users to develop complex high performance FPGA Computing applications more easily, reducing risk, cost and shortening time to market.

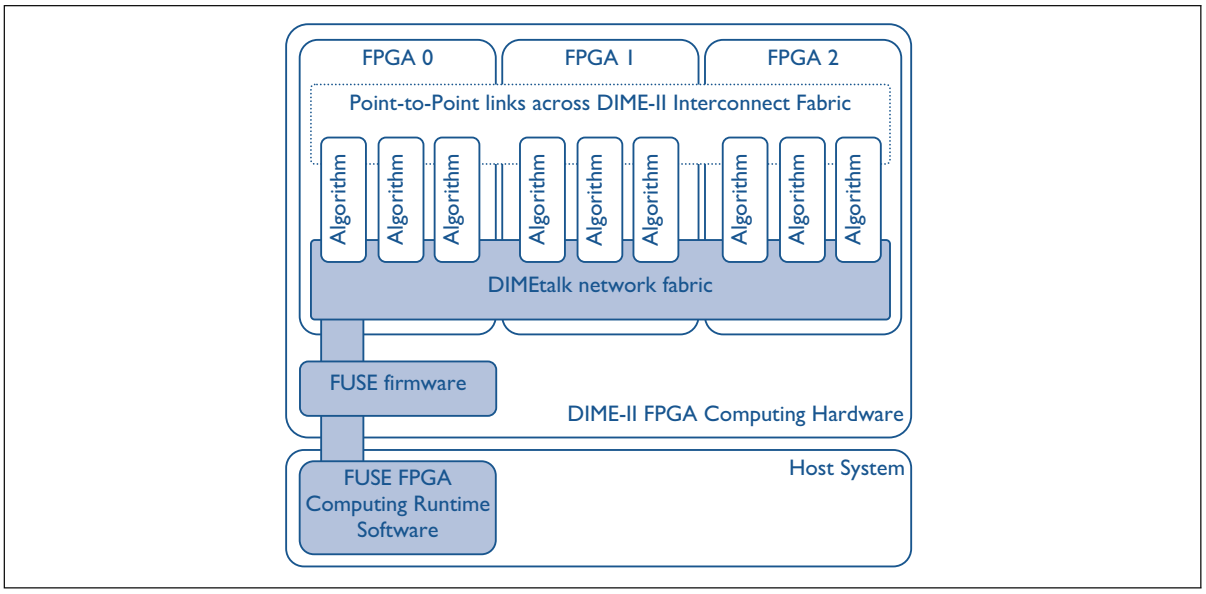


Figure 1: DIMEtalk in FPGA System

1.1.3 DIMEtalk Components

Once a user is familiar with how DIMEtalk works within an FPGA system it is important to consider the components which make up a DIMEtalk network. Data networks are a well established way of communicating data around systems yet many existing networking standards are overly cumbersome and overhead-heavy for use in FPGA systems. The simple network design and low overhead of DIMEtalk has been developed specifically for communications within FPGAs and between FPGAs in close proximity. Interfaces to longer distance and backplane interfaces mean that DIMEtalk can be used in conjunction with these standards. DIMEtalk networks are composed of four categories of underlying network components which the user can build together as required, to form the network on an application-specific basis. The components are FPGA IP blocks, available through the software tool, DIMEtalk System Design, and are shown in Table 2.

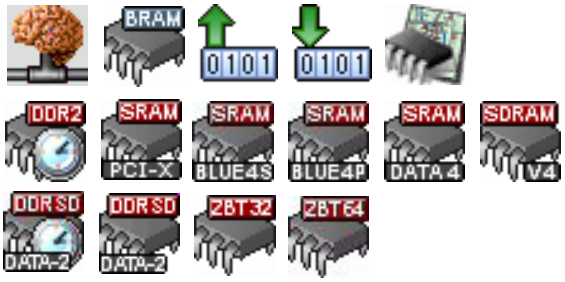
Generic Symbol	Description	DIMEtalk System Design Symbol
R	*Routers* direct data around the network and interconnect all other component types within a physical device.	
B	*Bridges* move data between physical devices across a defined physical media (i.e. between FPGAs).	
N	*Nodes* are the user interface to the network and can be connected to User FPGA designs via node interfaces (Block RAM,SRAM, DDR SDRAM, ZBT, FIFO, Memory Map).	
E	*Edges* interface the network to/from another data transfer standard (such as PCI, PCI-X,VME, Ethernet or USB on Nallatech cards).	

Table 2: DIMEtalk Components

Figure 2 shows how these components can be used in an example multiple FPGA network on Nallatech hardware (BenNUEY motherboard, BenDATA and BenADDA modules). The role of each network component is explained below.

1. The *Edge* component allows the network to interface with the PCI FPGA.
2. The *Router* receives data from its edge component. Routers pass data around the network and connect all the component types within the device.
3. The *Router* passes data to *Nodes* which are the user interface to the network.

CD_Drive:\ autorun.exe. In the DIMEtalk menu which appears, click on '**Install DIMEtalk Design Tools**'.

2. The DIMEtalk setup wizard appears. Work through the series of dialog boxes until the 'Finish' box is reached.

3. Click '**Finish**' to install the software.

2.2 Building a DIMEtalk Network

This section describes how to create an initial DIMEtalk network and provides an introduction to the tool and its various components. This initial example can be used to explore the various options in the DIMEtalk System Design toolbar and menus, and to become familiar with the network creation process. Figure 4 shows a simple network in the DIMEtalk System Design tool containing a node, a router and an edge. Note that the exact order of the component tabs are configurable so they may not look the same between different systems.

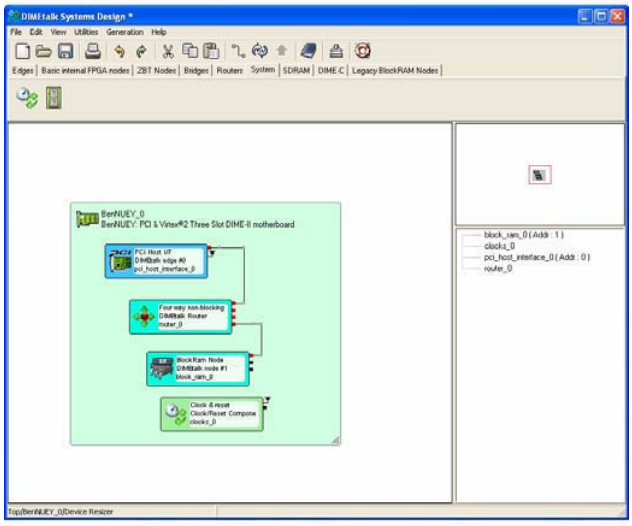


Figure 4: Initial DIMEtalk Network

Figure 5 shows how these components (node, router edge) relate to the physical hardware used - in this case a BenNUEY-PCI motherboard

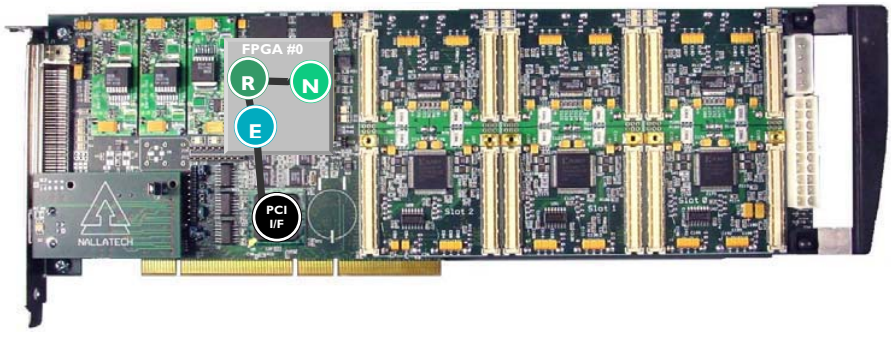


Figure 5: Initial DIMEtalk Network Projected onto Hardware