DIMEtalk 3.1 User Guide

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**Contents**

**About this User Guide** ........................................................................................................... xi

**Part I: Introduction** ................................................................................................................ 1

  DIMEtalk Overview .................................................................................................................. 3
  DIMEtalk Key Features ............................................................................................................ 3
    Introduction ............................................................................................................................... 3
    How DIMEtalk Works Within a Nallatech FPGA Computing System ......................... 4
    DIMEtalk Components ......................................................................................................... 4
    Building and Managing DIMEtalk Networks ................................................................. 6

**Getting Started** .................................................................................................................... 9

  Installation ...................................................................................................................................... 9

  Host System Requirements ..................................................................................................... 9

  Building a DIMEtalk Network ............................................................................................ 10

**Part II: DIMEtalk Implementation** .................................................................................. 19

  Using DIMEtalk ........................................................................................................................... 21

    DIMEtalk System Design - Designing a DIMEtalk Network ............................................ 22
      Overview .................................................................................................................................... 22
      Starting DIMEtalk System Design ......................................................................................... 22
      Toolbars, Tabs and Menus ..................................................................................................... 23
      DIMEtalk System Design Tool ............................................................................................. 26
      DIMEtalk Component Library Manager .............................................................................. 26

    DIMEtalk Components .......................................................................................................... 27
      What are Components? .......................................................................................................... 27
      Adding Components .............................................................................................................. 27
      Connecting Components .................................................................................................... 28
      Manipulating Components ................................................................................................. 29
      Using the Component Editor ............................................................................................... 29

    DIMEtalk Devices ..................................................................................................................... 30
      What are Devices? ................................................................................................................... 30
      Assigning Components to a Device ..................................................................................... 30
      Using the Device Editor ....................................................................................................... 31

    Connectivity and Constraints ............................................................................................ 33
      Adding Signal Breakouts ...................................................................................................... 33
      Creating a Bus Connection ................................................................................................ 33
      Creating Subsystems ......................................................................................................... 33
      Adding Notes ...................................................................................................................... 34
      Using Clocks within DIMEtalk .......................................................................................... 35
Code Generation ......................................................................................................................36
Generating VHDL Files ........................................................................................................... 36
Files Created during VHDL Generation ............................................................................. 37
Creating a Xilinx Project Navigator File ......................................................................... 38
DIMEtalk Tutorials ..................................................................................................................39
Connecting Signals to External Pins - a tutorial .......................................................40
Using the DIMEtalk Library Manager - a tutorial .....................................................44
List of Figures

Figure 1:DIMEtalk in FPGA System...........................................................................................................4
Figure 2:Example Multiple-FPGA Network ..............................................................................................6
Figure 3:DIMEtalk System Design...........................................................................................................6
Figure 4:Initial DIMEtalk Network............................................................................................................10
Figure 5:Initial DIMEtalk Network Projected onto Hardware ...................................................................10
Figure 6:PCI Edge.......................................................................................................................................11
Figure 7:Router Component.......................................................................................................................12
Figure 8:Block RAM Component...............................................................................................................12
Figure 9:Edit Block RAM Memory Address Width ..................................................................................13
Figure 10:Wired Network...........................................................................................................................13
Figure 11:Create a Device..........................................................................................................................14
Figure 12:Device Selection........................................................................................................................14
Figure 13:Device Type.................................................................................................................................15
Figure 14:Resize BenNUEY-PCI Device .....................................................................................................15
Figure 15:Clock & Reset Component ........................................................................................................16
Figure 16:Save Network..............................................................................................................................16
Figure 17:Compilation Button..................................................................................................................17
Figure 18:Build Network............................................................................................................................17
Figure 19:Warnings and Error..................................................................................................................18
Figure 20:DIMEtalk System Design Editor ............................................................................................22
Figure 21:DIMEtalk System Design Toolbar ..........................................................................................23
Figure 22:DIMEtalk System Design Tabs ...............................................................................................23
Figure 23:Document in HTML................................................................................................................25
Figure 24:DIMEtalk System Design Workspace ....................................................................................26
Figure 25:DIMEtalk Component Library Manager ................................................................................26
Figure 26:Add a Component.....................................................................................................................27
Figure 27:Connect Components................................................................................................................28
Figure 28:Component Manipulation..........................................................................................................29
Figure 29:Component Editor.....................................................................................................................29
Figure 30:Assign Components..................................................................................................................31
Figure 31:Assigning Signals to Pins ..........................................................................................................31
Figure 32:Open the Constraint Editor .....................................................................................................32
Figure 33:Drag Signals onto Pins..............................................................................................................32
Figure 34:Signal Breakout..........................................................................................................................33
Figure 35:Creating a Bus Connection .......................................................................................................33
Figure 36:Subsystem..................................................................................................................................34
Figure 37:Add a Note.................................................................................................................................34
Figure 38:Note added in DIMEtalk System Design ...............................................................................34
Figure 39:Clock Driver Module Component - External .........................................................................35
Figure 40:Clock Driver Module Component - Internal ..........................................................................35
Figure 41:Tcl File to Build Application...................................................................................................36
Figure 42: Warnings and Errors
Figure 43: Files Created During VHDL Generation
Figure 44: Lock Signal
Figure 45: DIMEtalk Device Editor
Figure 46: Constraint Editor
Figure 47: ‘lock’ signal dragged to ‘led[1]’ pin
Figure 48: lock connected to led[1]
Figure 49: Constraints File created for BenNUEY_0
Figure 50: UCF Showing Constrained Signal
Figure 51: Library Manager Button
Figure 52: Moving Components within Library Manager
Figure 53: Make Component Tab Invisible
Figure 54: Make Individual Components Invisible
Figure 55: Edit Block RAM Component
Figure 56: Component Editor
Figure 57: Signals Tab in Component Editor
Figure 58: Support Files Tab in Component Editor
Figure 59: Parameters Tab in Component Editor
Figure 60: Edit constraints for pci_host_interface
Figure 61: Component Constraints tab in Component Editor
List of Tables

Table 1: FUSE Naming Conventions ........................................................................................................... xiii
Table 2: DIMEtalk Components ..................................................................................................................... 5
Table 3: DIMEtalk Menus ............................................................................................................................... 24
Table 4: DIMEtalk File Descriptions ............................................................................................................. 37
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About this User Guide

Using this manual

This User Guide provides information on using DIMEtalk. The manual is designed to provide information for users of DIMEtalk to become acquainted with the tool, its features and the functionality it provides. After reading the introduction you should proceed with the getting started section which describes how to install DIMEtalk and how to build a simple network. The implementation section describes in detail how to use the DIMEtalk interface and contains information on components, devices, connectivity and code generation. Several example tutorials are also detailed.

- For information on individual DIMEtalk components and data packet structure see the DIMEtalk Reference Guide.
- For additional application notes please visit www.nallatech.com/applicationnotes.
- For information on using the DIMEtalk Application Program Interface (API) see the FUSE C-C++ API Developer's Guide.

Symbols Used

Throughout this manual there are symbols to draw attention to important information:

▼ The red arrow symbol indicates a set of procedures to follow, such as installing software or setting up hardware.

The blue ‘i’ symbol indicates useful or important information.

The red ‘!’ symbol indicates a warning, which requires special attention.

User Guide Format

The User Guide is divided into Sections, which are grouped into Parts. The parts divide the document as follows:

- Introduction: Provides an overview of DIMEtalk and its key components plus a getting started section which details how to build an example network.
About this User Guide

- DIMEtalk Implementation: How to start using DIMEtalk System Design including a description of DIMEtalk components, devices, connectivity and code generation. Example tutorials are also detailed.

Related Nallatech Documentation

- Nallatech DIMEtalk Reference Guide
- Nallatech FUSE C-C++ API Developer’s Guide
- Nallatech FUSE System Software User Guide
- Nallatech Tcl Plug-In for FUSE Developer’s Guide

Abbreviations

- API: Application Program Interface
- DAC: Digital-to-Analog Converter
- DIME: DSP and Image Processing Modules for Enhanced FPGAs
- FIFO: First In First Out stack memory
- FIR: Finite Impulse Response
- FPGA: Field Programmable Gate Array
- FUSE: Field Upgradeable System Environment
- IDE: Integrated Development Environment
- I/O: Input/Output
- PCI: Peripheral Component Interconnect
- SRAM: Static Random Access Memory
- UCF: User Constraints File
- USB: Universal Serial Bus
- VHDL: VHSIC Hardware Description Language

Typographical Conventions

The following typographical conventions are used in this manual:

- **Red text** indicates a cross-reference to information within the document set you are currently reading. Click the red text to go to the referenced item. To return to the original page, right-click anywhere on the current page and select Go To Previous View.
- **Blue underlined text** indicates a link to a Web page. Click blue-underlined text to browse the specified Web site.
- **Italics** denotes the following items:
  - References to other documents:
    - See the FUSE System Software User Guide for more information.
  - Emphasis in text:
    - Enable Loopback should not be enabled until all other registers have been set up.
FUSE Naming Conventions

Please note that the DIMEtalk clocks are named differently in the FUSE System Software compared to this User Guide. The clock naming conventions are shown in Table 1.

<table>
<thead>
<tr>
<th>Clock Names in FUSE</th>
<th>Clock Names in Documentation</th>
</tr>
</thead>
<tbody>
<tr>
<td>System Clock (SYSCLK)</td>
<td>Clock A (CLK A)</td>
</tr>
<tr>
<td>DSP Clock (DSPCLK)</td>
<td>Clock B (CLK B)</td>
</tr>
<tr>
<td>Pixel Clock (PIXCLK)</td>
<td>Clock C (CLK C)</td>
</tr>
</tbody>
</table>

Table 1: FUSE Naming Conventions

Comments and Suggestions

At the back of this User Guide, you will find a remarks form. We welcome any comments you may have on our product or its documentation. Your remarks will be examined thoroughly and taken into account for future versions of Nallatech products.
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Part I: Introduction

This part of the User Guide provides an overview of DIMEtalk and describes how to install the software and build a simple network.
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Section 1

DIMEtalk Overview

In this section:

• DIMEtalk Key Features

1.1 DIMEtalk Key Features

1.1.1 Introduction

DIMEtalk enables developers to design packet-based communications networks across multiple FPGAs. These networks are then provided to the user through an automatic code generation mechanism for deployment within their application design. DIMEtalk extends the capability of Nallatech cPCI, VME, PCI, PCI-X and PCI-104 COTS FPGA computing systems. This functionality offers a proven COTS solution, designed for ease of use, low risk system integration/in-field deployment. Some of DIMEtalk’s key features include:

• Powerful tool for designing and deploying embedded communications networks within FPGA systems.
• Networks provide integrated communication between user algorithm blocks in multiple FPGAs and the host system (VME, cPCI, etc).
• Intuitive GUI software interface for network design.
• Drag and Drop User Constraints (UCF) editing for Nallatech hardware.
• Automatic synthesizeable VHDL code generation.
• Supports Xilinx, Virtex-II, Virtex-II Pro, Virtex-E and Virtex-4.
• Low FPGA resource requirements.
• Directly supports all Nallatech DIME-II hardware products.
• Dedicated DIMEtalk FUSE API functions - C/C++/Tcl".  

1. These functions can be found in the FUSE C-C++ API Developer’s Guide.
1.1.2 How DIMEtalk Works Within a Nallatech FPGA Computing System

Figure 1 shows how DIMEtalk abstracts the features of the hardware platform to provide an easy to use development environment for implementing applications on multi-FPGA systems. Standard VHDL design flows are complemented with support for third-party compiler tools alongside an integrated C to VHDL Function Generator, DIMEC, enabling developers to select the design flow most appropriate to their application.

Communications networks between algorithm blocks, memory and I/O interfaces can be rapidly created across multiple FPGAs through the GUI-based application development environment. This functionality enables users to develop complex high performance FPGA Computing applications more easily, reducing risk, cost and shortening time to market.

![Figure 1: DIMEtalk in FPGA System](image)

1.1.3 DIMEtalk Components

Once a user is familiar with how DIMEtalk works within an FPGA system it is important to consider the components which make up a DIMEtalk network. Data networks are a well established way of communicating data around systems yet many existing networking standards are overly cumbersome and overhead-heavy for use in FPGA systems. The simple network design and low overhead of DIMEtalk has been developed specifically for communications within FPGAs and between FPGAs in close proximity. Interfaces to longer distance and backplane interfaces mean that DIMEtalk can be used in conjunction with these standards. DIMEtalk networks are composed of four categories of underlying network components which the user can build together as required, to form the network on an application-specific basis. The components are FPGA IP blocks, available through the software tool, DIMEtalk System Design, and are shown in Table 2.
Table 2: DIMEtalk Components

<table>
<thead>
<tr>
<th>Generic Symbol</th>
<th>Description</th>
<th>DIMEtalk System Design Symbol</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>Routers direct data around the network and interconnect all other component types within a physical device.</td>
<td>![Routers Symbol]</td>
</tr>
<tr>
<td>B</td>
<td>Bridges move data between physical devices across a defined physical media (i.e. between FPGAs).</td>
<td>![Bridges Symbols]</td>
</tr>
<tr>
<td>N</td>
<td>Nodes are the user interface to the network and can be connected to User FPGA designs via node interfaces (Block RAM, SRAM, DDR SDRAM, ZBT, FIFO, Memory Map).</td>
<td>![Nodes Symbols]</td>
</tr>
<tr>
<td>E</td>
<td>Edges interface the network to/from another data transfer standard (such as PCI, PCI-X, VME, Ethernet or USB on Nallatech cards).</td>
<td>![Edges Symbols]</td>
</tr>
</tbody>
</table>

**Figure 2** shows how these components can be used in an example multiple FPGA network on Nallatech hardware (BenNUEY motherboard, BenDATA and BenADDA modules). The role of each network component is explained below.

1. The Edge component allows the network to interface with the PCI FPGA.
2. The Router receives data from its edge component. Routers pass data around the network and connect all the component types within the device.
3. The Router passes data to Nodes which are the user interface to the network.
4. Bridges move the data between devices.

1.1.4 Building and Managing DIMEtalk Networks

Once the components which comprise a DIMEtalk network are understood the next stage is to start building a network using the software. The DIMEtalk System Design tool allows a user to manage and configure the basic blocks to form complex and useful networks with little input required. Network component type, quantity and location are defined within each FPGA to meet the requirements of the end application. This tool can be accessed through the windows start menu by selecting 'Start > Programs > Nallatech > DIMEtalk Design Tools' and 'DIMEtalk System Design' which brings up the DIMEtalk System Design tool as shown in Figure 3. Full instructions on how to use the tool are provided later in this manual.

Having defined the network, user blocks of design (VHDL or VHDL-wrapped source) can be imported and interconnected to the network in the DIMEtalk System Design tool. FPGA I/O ports for the whole design can be mapped to the device pins, using the high-level drag and drop Device Editor. VHDL code and user constraints files for the network are then automatically generated by DIMEtalk System Design. This code can then be added with additional user designs and code if necessary, before being compiled using standard synthesis and implementation tools.

Figure 2: Example Multiple-FPGA Network

Figure 3: DIMEtalk System Design
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Section 2

Getting Started

In this section:

- Installation
- Building a DIMEtalk Network

2.1 Installation

2.1.1 Host System Requirements

The following minimum system requirements are recommended for the DIMEtalk host PC:

- Pentium III 800 MHz or equivalent
- 128MB RAM
- 200MB Hard Disk
- Windows™ 2000/XP operating system
- 1024 x 768 pixels screen resolution, 16-bit color
- Display setting 96dpi
- Xilinx ISE 7.1 service pack 4 Foundation tools (for bitstream generation)
- FUSE for Windows v2.18.2
- Macromedia Flash Player (for interactive tutorials)
- Web Browser
- Administrator privileges on the system
- System language set to English

DIMEtalk may also operate under Linux using the WINE application interface layer. Please note however that this option is not supported by Nallatech.

To install DIMEtalk on Windows 2000/XP use the following procedures:

1. Insert the supplied DIMEtalk installation CD into the system’s CD-ROM drive and wait for the CD to autorun. If autorun does not start click ‘Start->Run’ from the taskbar and run the following program:

---

1. For the H101 series components ISE 8.2 or above is the only supported ISE release.
Getting Started

**CD_Drive:\ autorun.exe.** In the DIMEtalk menu which appears, click on 'Install DIMEtalk Design Tools'.

2. The DIMEtalk setup wizard appears. Work through the series of dialog boxes until the ‘Finish’ box is reached.

3. Click ‘Finish’ to install the software.

### 2.2 Building a DIMEtalk Network

This section describes how to create an initial DIMEtalk network and provides an introduction to the tool and its various components. This initial example can be used to explore the various options in the DIMEtalk System Design toolbar and menus, and to become familiar with the network creation process. Figure 4 shows a simple network in the DIMEtalk System Design tool containing a node, a router and an edge. Note that the exact order of the component tabs are configurable so they may not look the same between different systems.

![Figure 4: Initial DIMEtalk Network](image)

Figure 4 shows how these components (node, router edge) relate to the physical hardware used - in this case a BenNUEY-PCI motherboard.

![Figure 5: Initial DIMEtalk Network Projected onto Hardware](image)
To build a new DIMEtalk network use the following procedures:

1. In the task bar select ‘Start > Programs > Nallatech > DIMEtalk Design Tools’ and ‘DIMEtalk System Design’ which brings up the DIMEtalk System Design tool. The first step is to choose a component. This enables a user to connect a network to the available host. In this case it is assumed that the motherboard is connected to a PCI bus. Therefore select the PCI component in the ‘Edges’ tab. Once the button is depressed, click in the window area below to insert this component. When a component is placed down the user is prompted to enter a name for it. Enter a name and click ‘OK’ as shown in Figure 6.

![Figure 6: PCI Edge](image)
2. At the heart of DIMEtalk networks are the routers which allow packets to move between various components in the network. Go to the 'Routers' tab to select the Router component and place it down in the network as shown in Figure 7.

![Figure 7: Router Component](image)

3. A functional node, in this case a block RAM component, should be placed down to ensure the network can be implemented properly. Go to the 'Basic internal FPGA internal nodes' tab and select the block RAM node as shown in Figure 8.

![Figure 8: Block RAM Component](image)

4. Once the block RAM node has been placed down there are certain parameters associated with the node which can be changed. For example the memory address width can be altered which changes the size of the memory created by the network. To do this right-click on the block RAM component in the
network and select 'Edit'. In the component editor go to the 'Parameters' tab and change the address width from 12 to 9 as shown in Figure 9. Changing this width from 12 to 9 creates a 512 word memory.

5. The components must now be wired together using the red terminals at the side of each component. Press the left mouse button when the cursor is over the red terminal on the right of the block RAM node. While holding the mouse button down, move the cursor over one of the red terminals on the right of the Router. When the cross cursor is directly over a red terminal, release the mouse button. A wire should appear connecting the two red terminals together. Repeat this step to wire the red terminal on the PCI Edge component to the Router. The network is now wired together as shown in Figure 10.
6. The device on which this network will reside must be defined. Right-click in free space and select ‘Create>Device’ from the menu which appears, as shown in Figure 11.

![Figure 11: Create a Device](image)

7. In the device selection window shown in Figure 12 select the BenNUEY-PCI motherboard and press ‘OK’.

![Figure 12: Device Selection](image)
8. Choose the device option from the list of supported options to insert a device into the design window as shown in Figure 13.

![Figure 13: Device Type](image1)

9. Once the BenNUEY-PCI device is placed down on the network it should be resized by dragging the resize handle in the bottom right hand corner to cover all the components as shown in Figure 14. This informs DIMEtalk that all these components are to be assigned to this device.

![Figure 14: Resize BenNUEY-PCI Device](image2)
10. All FPGA devices need a component to handle clocking and resets. Go to the 'System' tab to select the Clock & Reset component and place it down on the device, then click on ‘OK’ as shown in Figure 15.

![Figure 15: Clock & Reset Component](image)

11. Before continuing further, the network should be saved. Click on the disk button (right) in the toolbar menu and save the network to an appropriate location as shown in Figure 16.

![Figure 16: Save Network](image)
12. The final stage is to compile the VHDL for the network. First press the Generate VHDL button (right), then click on ‘Save’ in the dialog box to create all the appropriate VHDL files as shown in Figure 17.

![Figure 17: Compilation Button](image)

13. A list of all the files created appears\(^1\). In order to build the network simply click on ‘Build’ to start the build process - this calls the Xilinx ISE tools.

![Figure 18: Build Network](image)

\(^1\) For a complete listing of these files and their functions please see Table 4.
14. When the script completes a report of how many warnings and errors have been produced is displayed, as shown in Figure 19. The DIMEtalk network is now built.

Figure 19: Warnings and Error

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Part II: DIMEtalk Implementation

This part of the User Guide provides detailed information on how to use DIMEtalk and its key component - DIMEtalk System Design. Two example tutorials are also provided here.
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Section 3

Using DIMEtalk

In this section:

• Designing a DIMEtalk Network
• DIMEtalk Components
• DIMEtalk Devices
• Connectivity and Constraints
• Code Generation
• Xilinx Project File
3.1 DIMEtalk System Design - Designing a DIMEtalk Network

3.1.1 Overview

In order to create a DIMEtalk network the required nodes must be specified on the various programmable logic devices in the system and connected to each other and the wider system. The tool provided for this process is DIMEtalk System Design, which enables the user to specify the location and type of all nodes, bridges, routers and interfaces used in the system. Once the network has been planned, DIMEtalk System Design can be used to autogenerate all the required VHDL files to create the design.

3.1.2 Starting DIMEtalk System Design

DIMEtalk System Design requires minimal memory and disk resources and runs under all Microsoft 32-bit Windows versions. DIMEtalk System Design can be started in two ways:

- Double-click on the DIMEtalk System Design desktop shortcut
  or
- Choose 'Start->DIMEtalk Design Tools->DIMEtalk System Design' from the Windows start menu

When the DIMEtalk System Design tool appears as shown in Figure 20 a previous design can be loaded using the Open File button (left) or by choosing 'File->Open' from the menu. A new network design can be created by clicking on the New Design button (right) or by selecting 'File>New' from the menu.

Figure 20: DIMEtalk System Design Editor
3.1.3 Toolbars, Tabs and Menus

Toolbar

The DIMEtalk System Design toolbar provides quick access to frequently used operations and commands. The toolbars used in DIMEtalk System Design are shown in Figure 21 with their functions listed.

Tabs

The tabs used in DIMEtalk System Design are shown in Figure 22.
# Menus

The menus available in DIMEtalk System Design provide the same functions as the standard tool bar with additional features such as the ability to save a design as an HTML file as well as other specific functions such as packaging up a design and zooming in on the navigator using the 'Navigator Zoom' menu. The menu contents are shown and explained in Table 3.

<table>
<thead>
<tr>
<th>Menu</th>
<th>Description:</th>
<th>Allows user to:</th>
</tr>
</thead>
</table>
| File menu | Create a new design | • create a new design  
• open an existing design  
• close a design  
• save a design  
• reopen a design, list recently open files in submenu  
• print the current view  
• document in HTML (see “Document a DIMEtalk Network in HTML” on page 25)  
• exit DIMEtalk |
| Edit menu | Undo last action | • undo last action  
• redo last undone action  
• cut an item  
• copy an item  
• paste an item  
• delete an item  
• select all items in DIMEtalk System Design tool |
| View menu | View Library Manager | • view Library Manager  
• refresh Library Manager  
• zoom in or out on the Navigator panel |
| Utilities menu | Package a design into one folder which stores all the components and XML files for the design, this allows user to move projects from one PC to another or archive them for later use | • package a design into one folder which stores all the components and XML files for the design, this allows user to move projects from one PC to another or archive them for later use |

Table 3: DIMEtalk Menus
As mentioned in the previous table DIMEtalk System Design enables the user to generate an interactive HTML document that describes their system. This shows all connections and components, allowing the user to share design information with others. For example, the DIMEtalk network which was created earlier produces the HTML files which are created and stored by default on C:\Program Files\Nallatech\DIMEtalk\projects\Examples\Simple Network.

Figure 23 shows these HTML files. For an overall view of the network click on the file named Top.html then click on the various network components as shown below to bring up the parameters, connections and support files for each component in the network - in this example the components include a block RAM node, PCI Edge, Router and Clock & Reset.

### Table 3: DIMEtalk Menus

<table>
<thead>
<tr>
<th>Menu</th>
<th>Description:</th>
<th>Allows user to:</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Design</strong></td>
<td>Generation menu</td>
<td>• generate network code</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• set Placer effort level&lt;sup&gt;a&lt;/sup&gt;</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• set Router effort level&lt;sup&gt;b&lt;/sup&gt;</td>
</tr>
<tr>
<td><strong>Help</strong></td>
<td>Help menu</td>
<td>• view Help contents</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• view information about DIMEtalk</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• view range of interactive tutorials</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• view Nallatech’s website</td>
</tr>
</tbody>
</table>

<sup>a</sup> The ‘Placer Effort’ option is passed through to the Place and Route process in the Xilinx ISE software. The Standard, Medium or High setting relates to how long an algorithm spends looking for a correct solution - the higher the setting the longer the time spent looking for a correct solution, and the higher the possibility of finding one.

<sup>b</sup> The ‘Router Effort’ option is passed through to the Place and Route process in the Xilinx ISE software. The Standard, Medium or High setting relates to how long an algorithm spends looking for a correct solution - the higher the setting the longer the time spent looking for a correct solution, and the higher the possibility of finding one.

### Document a DIMEtalk Network in HTML

As mentioned in the previous table DIMEtalk System Design enables the user to generate an interactive HTML document that describes their system. This shows all connections and components, allowing the user to share design information with others. For example, the DIMEtalk network which was created earlier produces the HTML files which are created and stored by default on C:\Program Files\Nallatech\DIMEtalk\projects\Examples\Simple Network.

Figure 23 shows these HTML files. For an overall view of the network click on the file named Top.html then click on the various network components as shown below to bring up the parameters, connections and support files for each component in the network - in this example the components include a block RAM node, PCI Edge, Router and Clock & Reset.

**Figure 23: Document in HTML**
3.1.4 DIMEtalk System Design Tool

Figure 24 shows the DIMEtalk System Design tool which displays the various components used to construct a DIMEtalk network. These include a block RAM node, a router, a PCI edge, and a Clock & Reset component, which are wired together to form a basic DIMEtalk network. Also highlighted are the tree view and navigation windows which provide alternative views of the created network.

3.1.5 DIMEtalk Component Library Manager

The Library Manager enables the user to customize the layout and appearance of the DIMEtalk design window. To open the Library Manager, shown in Figure 25, click on the Library Manager button (right) in the toolbar or select ‘View>Library Manager’ from the menu.
For an example of using the Library Manager please see "Using the DIMEtalk Library Manager - a tutorial".

3.2 DIMEtalk Components

This section provides an introduction to the components of DIMEtalk and how they can be used to create and manipulate networks. For more detailed descriptions of the specific components please see the DIMEtalk Reference Guide.

3.2.1 What are Components?

Components are the building blocks which are combined to make up a DIMEtalk network. They consist of routers, nodes, bridges and edges.

- Utility components are used to support the other components on hardware, managing clocking, grounding and resets.
- Routers direct data around the network.
- Nodes are the user interface to the network and can be connected to user application designs.
- Bridges move data between physical devices across a defined physical media (for example between FPGAs).
- Edges are a special type of node that indicate data entering/leaving the network from another data transfer standard (such as PCI, Ethernet, USB on Nallatech systems).
- Test components allow users to check that nodes are functioning properly. These components consist of a FIFO Test Loopback and a Memory Map Loopback.
- User components can be added into a DIMEtalk network. These components include the externally generated VHDL component and previously created DIMEtalk components.
- Testbench components allow users to simulate devices in order to test networks in simulation tools (i.e. ModelSim).

3.2.2 Adding Components

The first stage in generating a DIMEtalk network is to add and connect the various communications components for the design. This is done in the DIMEtalk System Design tool.

▼ To add a component to a DIMEtalk network use the following procedures:

1. In the DIMEtalk System Design tool select a component from one of the component tabs.
2. Click in the design space to place the component down. The component is then displayed (shown in Figure 26).

![Figure 26: Add a Component](image)
3.2.3 Connecting Components

To connect components in a DIMEtalk network use the following procedures:

1. In the DIMEtalk System Design tool move the cursor to the terminal of the first component.
2. When the cursor turns into a cross press the left-hand mouse button.
3. Move the cursor to the terminal of the other component, keeping the mouse button pressed when joining components.
4. When the cursor turns into a cross and the name of the component appears, release the mouse button to join the two components. To put an ‘elbow’ in a wire click on one of the dots on the wire and drag the wire to the appropriate place as shown in Figure 27.

At any point during the creation of a DIMEtalk network changes can be made using the ‘Edit>Undo’, ‘Edit>Redo’ menu commands. Also note that a network can be saved using the ‘File->Save’ menu command. If a design is closed without being saved, DIMEtalk prompts the user to save the network.
3.2.4 Manipulating Components

DIMEtalk components can be manipulated using the right-click menu, shown in Figure 28, which is displayed when a network component is right-clicked in the DIMEtalk System Design tool. The function of each menu item is also listed in the following figure.

![Figure 28: Component Manipulation](image)

3.2.5 Using the Component Editor

The component editor, shown in Figure 29 gives complete details of the DIMEtalk component and allows a user to alter the clocks and resets. It is accessed by right-clicking on a component in DIMEtalk. The component editor is split into five tabs which provide different information about the component.

![Figure 29: Component Editor](image)

**General Tab**

This tab shows details of the selected component and identifies it through a short and full description, its type and its location.
Signals Tab
The ‘Signals’ tab shows the external interface to the component. This tab can be used to alter the default connection for signals and resets. For example, right-click on dt_clk connected to CLKA and choose ‘Set Group Type>Clock>Clock B’ from the menus.

Support Files Tab
The ‘Support Files’ tab shows all the files that are required for any design using this component. These include the firmware parts of the component, additional software and documentation. Double-click on any file to open it using the default filetype handler on the development machine.

Parameters Tab
This tab contains the generics defined by the component. Some of these are editable - for example the size of new FIFO components can be set here.

Component Constraints Tab
This tab shows the various constraints which are placed on a component.

Instance Constraints Tab
This tab shows the constraints which are placed on a particular instance of a component. Note that any values the user enters for the instance constraints override the component constraints.

3.3 DIMEtalk Devices

3.3.1 What are Devices?
Devices represent the physical hardware deployed within a DIMEtalk network and are linked together by components. This hardware includes:

- BenONE, BenONE-PCI-104, BenERA, BenNUEY-PCI, BenNUEY-PCI-104, BenNUEY-4E, BenNUEY-PCI-X and BenNUEY-VME motherboards.
- BenADDA, BenBLUE-II, BenBLUE-III, BenBLUE-V4, BenDATA-II, BenDATA-V4, BenDATA-DD, BenDATA-WS, BenHOTLINK and BenPRO modules.
- XtremeDSP Development Kit.

3.3.2 Assigning Components to a Device

▼ To assign a component to a device use the following procedures:

1. Right-click on a component or in the design space to open the menu.

2. Select ‘Create Device’ from the right-click menu.
3. In the dialog box (shown in Figure 30) select the device required for the design. Click ‘OK’ on the relevant motherboard or module which displays a build option menu showing the FPGA speed grades and package types available for the hardware.

![Figure 30: Assign Components](image)

4. The device should now appear in the design tool as a green box which can be dragged over the components in the network as shown in “Building a DIMEtalk Network”. This places all the components into that device.

3.3.3 Using the Device Editor

The Device Editor allows a user to map the nets in a design onto physical pins by dragging the unassigned nets onto the appropriate pins. The list of nets comes from the connections that were wired to the top level in the design. The Device Editor is accessed by right-clicking on a device and selecting ‘Edit’ from the menu.

Assigning Signals

The principle function of the Device Editor is to assign signals to pins - this is done using the Constraint Editor function within the Device Editor. The following example shows how to assign LED signals to the pins of a block RAM node. Firstly the user should select the block RAM node, right-click on the lower black terminal (block RAM doorbell port) and select ‘Wire up a level’. Then right-click on the device and select ‘Edit’ to open the Device Editor as shown in Figure 31.

![Figure 31: Assigning Signals to Pins](image)
Using DIMEtalk

With the Device Editor open go to the right-hand Device Information pane and double-click on ‘blockram_1024_0’ as shown in Figure 32.

![Figure 32: Open the Constraint Editor](image)

This opens the Constraint Editor where the LED signals should be dragged from the ‘Off chip signals’ pane onto the correct pins in the ‘Available Pins’ pane as shown in the left hand image in Figure 33. The signals are now assigned to the relevant pins and the constraints appear in the lower pane under Non-default constraints. The right hand image in the Figure 33 shows these constraints.

![Figure 33: Drag Signals onto Pins](image)

**Automapping**

DIMEtalk automatically maps some signals to pins. Auto mapping is done on 4-bit bridges, all edges, clock & reset components and ZBT components (when wired up to the top level).
3.4 Connectivity and Constraints

3.4.1 Adding Signal Breakouts

This feature allows a user to breakout the signals within a connection group.

▼ To add a signal breakout use the following procedures:

1. Right-click on a component’s red terminal port.
2. Select ‘Create>Breakout’ from the menu which appears.
3. The signal breakout is now placed down in the DIMEtalk System Design tool as shown by the red arrow in Figure 34.

![Figure 34: Signal Breakout](image)

3.4.2 Creating a Bus Connection

This option appears on the right-click ‘Create’ submenu if the terminal contains only output signals. Unlike the signal breakout which gives one terminal per signal, all the terminals on a bus have the same signals as the initial terminal. Bus connections provide a way of connecting one terminal to multiple locations.

▼ To create a bus connection use the following procedures:

1. Right-click on a component’s terminal.
2. Select ‘Create>Bus’ from the menu which appears.
3. The bus is now placed down in the DIMEtalk System Design tool as shown by the red arrow in Figure 35.

![Figure 35: Creating a Bus Connection](image)

3.4.3 Creating Subsystems

When using the software it may be necessary to create larger, more complex networks. The ‘Create>Subsystem’ option allows a user to compartmentalize a design and make it more manageable.
To create a subsystem use the following procedures:

1. Select one or more components.
2. Select ‘Create>Subsystem’ from the menu which appears.
3. The subsystem (shown in Figure 36) is placed down in the tool and the component is now held within the subsystem.

4. Alternatively, a subsystem can be created by dragging a selection box over a number of components then right-clicking on one. All components are then placed into the subsystem.

3.4.4 Adding Notes

An additional function in the DIMEtalk System Design tool is the ability to add notes to a network. These can serve a variety of purposes - for example users designing large complex networks can deploy them as reference points in the network or reminders to complete a task at a certain point in the network.

To add a note to a network use the following procedures:

1. Right-click on a component.
2. Select ‘Create>Note’ from the menu which appears.
3. In the box (shown in Figure 37) enter the name for the note and click on ‘OK’.

4. The note can now be seen in the DIMEtalk System Design tool (shown in Figure 38).
3.4.5 Using Clocks within DIMEtalk

In the System tab when a user clicks on the Clock Driver Module (shown right), a module is created in DIMEtalk to handle the clocking of the other components within the module. Figure 39 shows how this component looks externally.

![Figure 39: Clock Driver Module Component - External](image)

Figure 40 shows an internal view of the component.

![Figure 40: Clock Driver Module Component - Internal](image)
There are no strict rules as to how the various clocks and resets can be used. However, by default:

1. DIMEtalk clock on all components is wired to be clk1.
2. DIMEtalk network reset on all components is wired to reset.
3. Host clock on relevant components (e.g. PCI Edge) is wired to clk2.
4. User clock on all components is wired to clk1.
5. Clk1 is assumed to be 100MHz, clk2 is assumed to be 40MHz, clk3 is assumed to be 100MHz.

These default wirings can be altered by opening a component and changing the connection. Note that DIMEtalk will not prevent potentially invalid connections e.g. half a DIMEtalk network on clk1 and half on clk2. In addition, the three clocks must be constrained to appropriate pins in the module (via the Device Editor). The general assumption is that clk1 will be wired to CLKA, clk2 to CLKB and clk3 to CLKC. Again, this is a suggested method which can be altered on the proviso that no checks are made as to the validity of any variation.

3.5 Code Generation

3.5.1 Generating VHDL Files

Once a network is created select the Generate Network code button (right) or choose ‘Generation>Generate Network Code’ from the drop-down menu. This prompts the user to select a top level directory where the network will be stored. A list of all the files created then appears, as shown in Figure 41, which contains a Tcl file to build the application. Double-click on this or click ‘Build’ to start the build process.

Figure 41: Tcl File to Build Application
When the script completes, a report of the warnings and errors produced is displayed as shown in Figure 42.

### 3.5.2 Files Created during VHDL Generation

Following VHDL Generation a number of files are created which have different functions within the DIMEtalk network. These files are highlighted in Figure 43 which shows how they appear in the software. The files created are also listed with their functions in Table 4.

![Figure 42: Warnings and Errors](image)

**Figure 43: Files Created During VHDL Generation**

<table>
<thead>
<tr>
<th>File Created</th>
<th>Description</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>dimetest.wish</td>
<td>Wish file</td>
<td>Load and test network (Wish script)</td>
</tr>
</tbody>
</table>

**Table 4: DIMEtalk File Descriptions**
Creating a Xilinx Project Navigator File

During the build process DIMEtalk creates a .ise project file. This enables the DIMEtalk network to be built using the Xilinx Project Navigator tool. It is possible to create this file without invoking the full build process by using a DOS command prompt as described below.

**To create the .ise file without invoking the full build process use the following procedures:**

1. In the task bar select ‘**Start > Accessories > Command Prompt >**’.
2. In the command prompt change directory into the top level directory where the network has been output and run the following command line:

   ```
   cd source\<Device name>
   ```

3. Followed by:

   ```
   tclsh build.tcl -ise
   ```

4. The .ise project should now be created in the device folder on the user's hard disk.
Section 4

DIMEtalk Tutorials

In this section:

- Connecting Signals to External Pins - tutorial
- Using the Library Manager - tutorial

The tutorials described in this section are also available as interactive demonstrations which walk-through each example and show the most appropriate methods for configuring and using DIMEtalk. The tutorials are installed on a system’s hard disk from the DIMEtalk installer to the location ‘<C:\Program Files\Nallatech\dimetalkdesign\DIMEtalk\help\tutorials>’ or from the menu in DIMEtalk System Design under ‘Help>Tutorials’. The tutorials require Flash Player in order to view them. Please visit http://www.macromedia.com/go/getflashplayer/ to download the latest Flash Player.

For information on other DIMEtalk features and applications please visit www.nallatech.com/applicationnotes.
4.1 Connecting Signals to External Pins - a tutorial

This tutorial shows how to assign specific signals to external physical pins through a DIMEtalk network. Signals that need to go to external pins are identified by DIMEtalk and largely routed automatically to appropriate pins. Occasionally however users may wish to route a non-essential signal to an external pin - for example the ‘lock’ signal of the Clock & Reset component.

To connect a signal to an external pin through DIMEtalk use the following procedures:

1. Load the network created in “Building a DIMEtalk Network”.

2. The Clock & Reset component has a ‘lock’ signal, shown in Figure 44, which indicates that all the clocks are operating correctly. For this tutorial the signal is brought out to an LED.

3. In order to make the ‘lock’ signal available for external wiring, right-click the black terminal at the side of the Clock and Reset component and select ‘Wire up a level’ from the menu. Right-click anywhere in the device to open the Device Editor. In the Device Editor go to the ‘Edit Devices’ tab and double-click on the ‘clocks_0’ component as shown in Figure 45.

Figure 44: Lock Signal
4. Double-click on the 'clocks_0' component to bring up the Constraint Editor, Figure 46, which shows five signals coming from the component to external pins. Four of these - three clocks and a reset - are already assigned to appropriate physical pins whilst the 'lock' signal is unassigned.

5. Scroll down the list of available pins on the right hand side until the set of LEDs appears. Drag the 'lock' signal onto the 'led[1]' pin as shown in Figure 47.
6. This creates a non-default constraint - constraining the ‘lock’ signal to a location known as ‘led[1]’.

7. Return to the Device Editor’s main window and in the ‘System View’ tab double-click on ‘Constrained Signals’ under the ‘BenNU5EY_0’ node. This opens the list of signals and displays the last entry as ‘lock connected to led[1]’. Click ‘OK’ to return to DIMEtalk System Design.

8. In DIMEtalk System Design click on the ‘Generate VHDL’ button then click on ‘Save’ in the dialog box to create all the appropriate VHDL files.

9. In Figure 49 the constraints file which has been created for the BenNU5EY_0 is highlighted. Double-click on this to open it.
10. This opens a UCF (User Constraints File), shown in Figure 50, which now displays the ‘lock’ signal constrained to the physical pin E3.

11. When this network is built LED1 on the BenNUEY-PCI motherboard will switch off as the active high lock signal is asserted on locking all of the clocks for the network.

12. The signal has now been connected to a physical pin through DIMEtalk.
4.2 Using the DIMEtalk Library Manager - a tutorial

This tutorial shows how to use the DIMEtalk Library Manager. The Library Manager is the part of DIMEtalk System Design that allows users to decide which components are available in the component tabs for use within networks.

▼ To open the DIMEtalk Library Manager use the following procedures:

1. In DIMEtalk System Design click on the Library Manager button in the toolbar as shown in Figure 51.

![Figure 51: Library Manager Button](image1)

2. In the Library Manager window drag a component folder - in this case ‘Basic internal FPGA’ nodes - to the top of the tree as shown in Figure 52. Close the Library Manager and in the DIMEtalk design window this tab now appears as the first tab.

![Figure 52: Moving Components within Library Manager](image2)

3. Entire tabs can also be made invisible using the Library Manager. For example, right-click on the ‘Basic internal FPGA nodes’ in the Library Manager and select ‘Make Invisible’ from the menu which appears, as shown in Figure 53. Close the Library Manager and in DIMEtalk System Design the ‘Basic internal FPGA nodes’ tab is no longer visible. To change this open the Library Manager again and click on the
Basic internal FPGA nodes' folder and select 'Make Visible' from the menu which appears. The tab is now visible again in the DIMEtalk design window.

4. Individual components can also be made invisible. In the Library Manager open the 'Basic internal FPGA nodes' folder, right-click on 'block RAM' and select 'Make Invisible' as shown in Figure 54.

5. In DIMEtalk System Design go to the 'Basic internal FPGA nodes' tab where the block RAM node is no longer visible. To change this open the Library Manager again, open the 'Basic internal FPGA nodes' folder and right-click on 'block RAM' to select 'Make Visible' from the menu which appears. Close the Library Manager and this component is now visible again in the 'Basic internal FPGA nodes' tab in DIMEtalk System Design.

6. In the Library Manager open the Basic internal FPGA nodes folder and select the block RAM component shown in Figure 55. Note that the location of the definition and the date on which it was saved are
shown under the component. Double-click on the block RAM component to open the Component Editor.

![Figure 55: Edit Block RAM Component](image)

7. The Component Editor window, shown in [Figure 56], provides some basic information about the component such as a full description, short description, and the type of component. Note that it is not possible to edit the identifier as this has to be unique within DIMEtalk.

![Figure 56: Component Editor](image)

8. The ‘Signals’ tab shows the external interface to the component. This tab can be used to alter the default connection for signals and resets. For example, right-click on ‘user_clk connected to CLKA’ and choose **Set Group Type>Clock>CLKB** from the menus as shown in [Figure 57]. This connects the DIMEtalk signal to Clock B.

![Figure 57: Signals Tab in Component Editor](image)
9. The Support Files tab, shown in Figure 58, displays all the files that are required for any design using this component. Click on ‘OK’.

![Figure 58: Support Files Tab in Component Editor](image)

10. The Parameters tab, shown in Figure 59, displays parameters which can alter a component’s behavior. Click on ‘OK’.

![Figure 59: Parameters Tab in Component Editor](image)

11. The final tab shows Component Constraints - in the case of the block RAM component there are none. For an example of constraints go back to the Library Manager and open the ‘Edges’ folder and double-click on ‘pci_host_interface’ as shown in Figure 60.

![Figure 60: Edit constraints for pci_host_interface](image)
12. This brings up the Component Editor again and Figure 61 shows the various signals constrained to the appropriate pins within a device. These constraints also include timing constraints against global clock resources.

Figure 61: Component Constraints tab in Component Editor
Standard Terms and Conditions

GENERAL
These Terms and Conditions shall apply to all contracts for goods sold or work done by Nallatech Limited. (hereinafter referred to as the "company" or Nallatech) and purchased by any customer (hereinafter referred to as the customer).

Nallatech Limited trading in the style Nallatech (the company), submits all quotations and price lists and accepts all orders subject to the following conditions of contract which apply to all contracts for goods supplied or work done by them or their employees to the exclusion of all other representations, conditions or warranties, express or implied.

The buyer agrees to execute and return any license agreements as may be required by the company in order to authorize the use of those licensable items. If the licensable item is to be resold this condition shall be enforced by the re-seller on the end customer.

Each order received by the company will be deemed to form a separate contract to which these conditions apply and any waiver or any act of non-enforcement or variation of these terms or part thereof shall not bind or prejudice the company in relation to any other contract.

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The company reserves the right to vary the specification or withdraw from the offer any of its products without prior warning.

The company reserves the right to refuse to accept any contract that is deemed to be contrary to the companies policies in force at the time.

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All prices shown on the company’s price list, or on quotations offered by them, are based upon the acceptance of these conditions. Any variation of these conditions requested by the buyer could result in changes in the offered pricing or refusal to supply.

All quoted pricing is in Pounds Sterling and is exclusive of Value Added Tax (VAT) and delivery. In addition to the invoiced value the buyer is liable for all import duty as may be applicable in the buyer’s location. If there is any documentation required for import formalities, whether or not for the purposes of duty assessment, the buyer shall make this clear at the time of order.

Quotations are made by Nallatech upon the customer’s request but there is no obligation for either party until Nallatech accepts the customer’s order.

Nallatech reserves the right to increase the price of goods agreed to be sold in proportion to any increase of costs to Nallatech between the date of acceptance of the order and the date of delivery or where the increase is due to any act or default of the customer, including the cancellation or rescheduling by the customer of part of any order.

Nallatech reserves the right (without prejudice to any other remedy) to cancel any uncompleted order or to suspend delivery in the event of any of the customer’s commitment with Nallatech not being met.

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All delivery times offered by the company are to be treated as best estimates and no penalty can be accepted for non compliance with them.

Delivery shall be made by the company using a courier service of its choice. The cost of the delivery plus a nominal fee for administration will be added to the invoice issued. Payment of all inward customs duties and fees are the sole responsibility of the buyer. If multiple shipments are requested by the buyer, multiple delivery charges will be made. In the case of multiple deliveries separate invoices will be raised.

If requested at the time of ordering an alternative delivery service can be used, but only if account details are supplied to the company so that the delivery can be invoiced directly to the buyer by the delivery service.

The buyer accepts that any 'to be advised' scheduled orders not completed within twelve months from the date of acceptance of the original order, or orders held up by the buyers lack of action regarding delivery, can be shipped and invoiced by the company and paid in full by the buyer, immediately after completion of that twelve month period.

INSURANCE
All shipments from the company are insured by them. If any goods received by the buyer are in an unsatisfactory condition, the following courses of action shall be taken.

If the outer packaging is visibly damaged, then the goods should not be accepted from the courier, or they should be signed for only after noting that the packaging has sustained damage.

If the goods are found to be damaged after unpacking, the company must be informed immediately.

Under no circumstances should the damaged goods be returned, unless expressly authorized by the company.

If the damage is not reported within 48 hours of receipt, the insurers of the company shall bear no liability.

Any returns made to the company for any reason, at any time shall be packaged in the original packaging, or its direct equivalent and must be adequately insured by the buyer.

Any equipment sent to the company for any purpose, including but not limited to equipment originally supplied by the company must be adequately insured by the buyer while on the premises of the company.

PAYMENT
Nallatech Ltd. terms of payment are 30 days net.
Any charges incurred in making the payment, either currency conversion or otherwise shall be paid by the buyer.
The company reserves the right to charge interest at a rate of 2% above the base rate of the Bank of Scotland PLC on any overdue accounts. The interest will be charged on any outstanding amount from said due date of payment, until payment is made in full, such interest will accrue on a daily basis.

**TECHNICAL SUPPORT**

The company offers a dedicated technical support via telephone and an E-mail address. It will also accept faxed support queries.

Technical support will be given free of charge for 90 days from the date of invoice, for queries regarding the use of the products in the system configuration for which they were sold. Features not documented in the user manual or a written offer of the company will not be supported. Interfacing with other products other than those that are pre-approved by the company as compatible will not be supported. If the development tools and system hardware is demonstrably working, no support can be given with application level problems.

**WARRANTY**

The company offers as part of a purchase contract 12 months warranty against parts and defective workmanship of hardware elements of a system. The basis of this warranty is that the fault be discussed with the companies technical support staff before any return is made. If it is agreed that a return for repair is necessary then the faulty item and any other component of the system as requested by those staff shall be returned carriage paid to the company. Insurance terms as discussed in the INSURANCE Section will apply.

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After warranty repair, goods will be returned to the buyer carriage paid by the company using their preferred method.

Faults incurred by abuse of the product (as defined by the company) are not covered by the warranty.

Attempted repair or alteration of the goods as supplied by the company, by another party immediately invalidates the warranty offered.

The said warranty is contingent upon the proper use of the goods by the customer and does not cover any part of the goods which has been modified without Nallatech's prior written consent or which has been subjected to unusual physical or electrical stress or on which the original identification marks have been removed or altered. Nor will such warranty apply if repair or parts required as a result of causes other than ordinary authorized use including without limitation accident, air conditioning, humidity control or other environmental conditions.

Under no circumstances will the company be liable for any incidental or consequential damage or expense of any kind, including, but not limited to, personal injuries and loss of profits arising in connection with any contract or with the use, abuse, unsafe use or inability to use the companies goods. The company’s maximum liability shall not exceed and the customers remedy is limited to, either:

i. repair or replacement of the defective part or product or at the companies option.

ii. return of the product and refund of the purchase price and such remedy shall be the customer’s entire and exclusive remedy.

Warranty of the software written by the company shall be limited to 90 days warranty that the media is free from defects and no warranty express or implied is given that the computer software will be free from error or will meet the specification requirements of the buyer.

The terms of any warranty offered by a third party whose software is supplied by the company will be honoured by the company exactly. No other warranty is offered by the company on these products.

Return of faulty equipment after the warranty period has expired, the company may at its discretion make a quotation for repair of the equipment or declare that the equipment is beyond repair.

**PASSING OF RISK AND TITLE**

The passing of risk for any supply made by the company shall occur at the time of delivery. The title however shall not pass to the buyer until payment has been received in full by the company. And no other sums whatever shall be due from the customer to Nallatech.

If the customer (who shall in such case act on his own account and not as agent for Nallatech) shall sell the goods prior to making payment in full for them, the beneficial entitlement of Nallatech therein shall attach to the proceeds of such sale or to the claim for such proceeds.

The customer shall store any goods owned by Nallatech in such a way that they are clearly identifiable as Nallatech's property. The customer will allow Nallatech to inspect these records and the goods themselves upon request.

In the event of failure by the customer to pay any part of the price of the goods, in addition to any other remedies available to Nallatech under these terms and conditions or otherwise, Nallatech shall be entitled to repossess the goods. The customer will assist and allow Nallatech to repossess the goods as aforesaid and for this purpose admit or procure the admission of Nallatech or its employees and agents to the premises in which the goods are situated.

**INTELLECTUAL PROPERTY**

The buyer agrees to preserve the Intellectual Property Rights (IPR) of the company at all times and that no contract for supply of goods involves loss of IPR by the company unless expressly offered as part of the contract by the company.

**GOVERNING LAW**

This agreement and performance of both parties shall be governed by Scottish law.
Any disputes under any contract entered into by the company shall be settled in a court if the company's choice operating under Scottish law and the buyer agrees to attend any such proceedings. No action can be brought arising out of any contract more than 12 months after the completion of the contract.

INDEMNITY
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<table>
<thead>
<tr>
<th>Topic</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>changing the default wirings</td>
<td>36</td>
</tr>
<tr>
<td>clock frequencies</td>
<td>36</td>
</tr>
<tr>
<td>DIMEtalk clock</td>
<td>36</td>
</tr>
<tr>
<td>DIMEtalk network reset</td>
<td>36</td>
</tr>
<tr>
<td>host clock</td>
<td>36</td>
</tr>
<tr>
<td>user clock</td>
<td>36</td>
</tr>
<tr>
<td>external view</td>
<td>35</td>
</tr>
<tr>
<td>internal view</td>
<td>35</td>
</tr>
<tr>
<td>using DIMEtalk</td>
<td>21</td>
</tr>
</tbody>
</table>
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Suggested Improvement

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