Figure 2-1. Cyclone II EP2C20 Device Block Diagram

Figure 2-2. Cyclone II LE
Figure 2-5. Cyclone II LAB Structure
Figure 2–8. R4 Interconnect Connections

Notes to Figure 2–8:
(1) C4 interconnects can drive R4 interconnects.
(2) This pattern is repeated for every IAR in the IAR row.
Figure 2-9. Register Chain Interconnects

- Local Interconnect Routing Among LEs in the LAB
- Carry Chain Routing to Adjacent LE
- Register Chain Routing to Adjacent LE's Register Input
Note to Figure 2-10:

(1) Each C4 interconnect can drive either up or down four rows.
Figure 2-17. M4K RAM Block LAB Row Interface

Direct link interconnect to adjacent LAB

Direct link interconnect from adjacent LAB

M4K RAM Block Local Interconnect Region

LAB Row Clocks

C4 Interconnects

R4 Interconnects
Figure 2-18. Multiplier Block Architecture

Note to Figure 2-18:
(1) If necessary, these signals can be registered once to match the data signal path.

Figure 2-19. Embedded Multiplier LAB Row Interface
Notes to Figure 2-21:

1) The 35 data and control signals consist of five data out lines, io_dataout[4..0], five output enables io_coe[4..0], five input clock enable, io_cce_in[4..0], five output clock enable, io_cce_out[4..0], five clocks, io_clk[4..0], five asynchronous clear signals, io_cce[4..0], and five synchronous clear signals, io_cclr[4..0].

2) Each of the five IOEs in the row I/O block can have two io_datain (combinatorial or registered) inputs.
Figure 2-22. Column I/O Block Connection to the Interconnect

Notes to Figure 2-22:
(1) The 28 data and control signals consist of four data out lines, io_data[3..0], four output enables, io_cce[3..0], four input clock enables, io_cci[3..0], four output clock enables, io_cce_out[3..0], four clocks, io_cclk[3..0], four asynchronous clear signals, io_cclr[3..0], and four synchronous clear signals, io_cscir[3..0].
(2) Each of the four IOEs in the column I/O block can have two io_datain (combinational or registered) inputs.